PMB 2520

Hammerhead

A-GPS Single-Chip Device

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Short Range Wireless

Global LOCATE™

Infineon technologies

Never stop thinking.

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PMB 2520

A-GPS Single Chip Device

Wireless Solutions

Never stop thinking.

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Revision History:2005-09-29T2520-XV10T7-7600

Previous Version: T2520-XV10T5-7600	
Section/ Figure	Subjects (major changes since last revision)
Chapter1	Added key performance figures
Chapter 5	Added interface timing

1 General Device Overview

The PMB 2520 Hammerhead GPS IC is Infineon Technologies and Global Locate´s next generation IC solution for GPS (Global Positioning System). The Hammerhead GPS single chip device enables the realization of a cost efficient GPS solution by integrating the complete radio frequency front-end as well as the signal processing functionality in a single die. The radio frequency front-end includes an LNA (low noise amplifier), VCO (voltage controlled oscillator), PLL (phase locked loop) and analog to digital converters. The PMB 2520 Hammerhead IC allows the usage of assistance data by supporting A-GPS (assisted GPS) standards (RRLP, RRC, OMA SUPL).

With the help of advanced digital signal processing techniques based on sophisticated correlation engines as well as powerful detection and navigation processing algorithms and the use of A-GPS data, the Hammerhead achieves enhanced sensitivity values of better than -158 dBm at the LNA input as is required for indoor applications. A sophisticated dynamic power management scheme supports several low-power modes which gives the lowest possible energy usage per fix.

The Hammerhead is especially targeted at the cellular market but it can also be used for automotive navigation and infotainment systems as well as the wireless PDA market segment. The main applications for Hammerhead are location based services and the localization of emergency calls for cellular systems according to, for example, the E911 mandate. In conjunction with the appropriate software and driver, integrated on the cellular host, the Hammerhead system realizes the complete functionality for mobile-assisted, mobile-based and/or autonomous GPS operation. By integrating the signal processing functionality the host system is relieved of all real-time critical A-GPS tasks.

One of three serial interfaces, UART, I²C or SPI, is used for communication with the host system. A JTAG interface for boundary scan is also available.

The device is fabricated in advanced semiconductor technology and is available in a PG-VQFN-48-4 package.

Feature Overview

General

- Single-chip A-GPS device for cellular applications and location based services, integrating the radio frontend and the GPS baseband on the same die
- Fabricated in advanced low-power 0.13µm CMOS technology
- Low power consumption using several power saving modes
- Supply from external voltage regulators or use the built in voltage regulators
- Advanced real time hardware correlator engine for enhanced sensitivity (better than -158 dBm at the LNA input for A-GPS)
- Fast Acquisition giving rapid Time-to-First-Fix (TTFF)
- Very low component count for lowest bill of material
- Multiple input clock signals supported
- Range of interface voltages supported
- Temperature range of -30 °C to +85 °C

Interfaces

- RF antenna input
- Serial full duplex UART interface
- Serial I^2C interface
- Serial full-duplex synchronous SPI interface
- IEEE 1149.1 compatible JTAG Test Access Port (TAP) and boundary scan

Software

- Hammerhead host software driver supports multiple mode operation (mobile-assisted, mobile-based and autonomous).
- Easy to use driver API

Type	Package
PMB 2520	PG-VQFN-48-4

1.1 Key performance specification

The specifications in this section are intended to provide guidance regarding typical system performance for cellular handsets utilizing the PMB 2520 Hammerhead. The achievable performance for a particular handset will vary depending upon RF environment and implementation.

The PMB2520 Hammerhead is designed to operate in networks without GPS timing, using approximate time provided through assistance data messages. The specifications below are inclusive of any degradations induced from timing errors of two seconds.

Table 1-1 Accuracy

Signal condition for all satellites	Circular Error Probability (CEP) accuracy	
	First Fix	Continuous Navigation
-130 dBm	10 m	2 m (note 1)
-150 dBm	20 m	10 m
-160 dBm	100 m (note 2)	50 m

Notes:
1. Atmospheric effects may degrade outdoor accuracy to 5m.
2. One satellite at -147dBm.

Table 1-2 Sensitivity

Type of fix	Minimum signal strength (signal condition for all Satellites)
Hot start (first fix after standby)	-160 dBm
First fix (MS-based or MS-assisted)	-154 dBm
First fix (Enhanced Autonomous)	-150 dBm
First fix (Autonomous)	-140 dBm

Table 1-3 Average power consumption

Signal condition for all satellites	
-130 dBm	70mW
-150 dBm	100mW
-130 dBm	25mW(note)

Note:
Low-power mode = 1Hz update rate with measurement time of 200ms

Table 1-4 Time To First Fix

Signal condition for all satellites	Time to first fix			
	Hot start (First Fix After Standby)	**First Fix** (Ms-based or MS-assisted)	**First Fix** (Autonomous)	**First Fix** (Enhanced Autonomous)
-130 dBm	1 s	1 s	60 s	15 s (note 1)
-140 dBm	2 s	2 s	60 s	
-150 dBm	6 s	10 s	-	30 s
-160 dBm	< 60 s	< 60 s (note 2)	-	-

Notes:
1. Enhanced Autonomous operation uses Global Locate's proprietary LTO file.
2. One satellite at -147dBm.

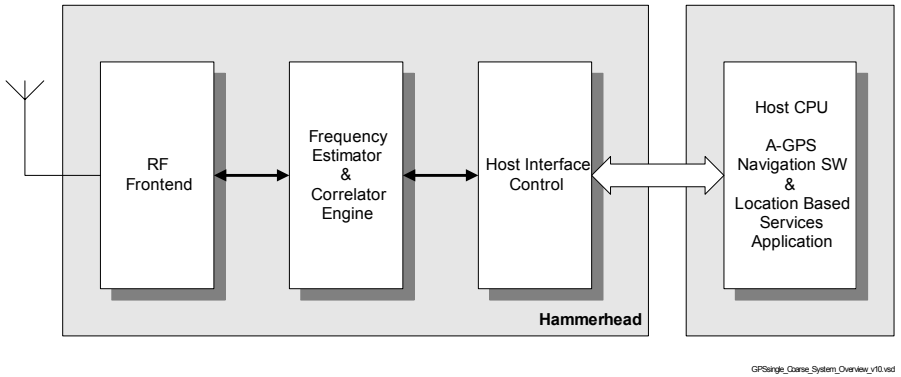
1.2 System Architecture Overview

Figure 1-1 shows a coarse block diagram of the complete GPS system architecture consisting of the PMB 2520 Hammerhead GPS IC and the host CPU. The Hammerhead is targeted mainly at cellular application like Location Based Services and the localization of emergency calls for cellular systems according to, for example, the E911 mandate. All the real-time critical signal processing for A-GPS operation is performed internally in the Hammerhead, removing any real-time loading from the system host CPU.

The corresponding host software allows for the operation of mobile-assisted and mobile-based A-GPS fully autonomous GPS and / or Global Locate patented Enhanced Autonomous. A flexible API (Application Programming Interface) is provided with the navigation software allowing an easy integration of the A-GPS functionality into e.g. a cellular protocol stack. No real-time interrupt service loading is added to the host system, thus considerably simplifying the system integration.

To support debug and production tests the PMB 2520 Hammerhead GPS IC contains a TAP controller. The TAP controller is compatible with the IEEE Standard Test Access and Boundary-Scan Architecture, IEEE Std 1149.1-2001.

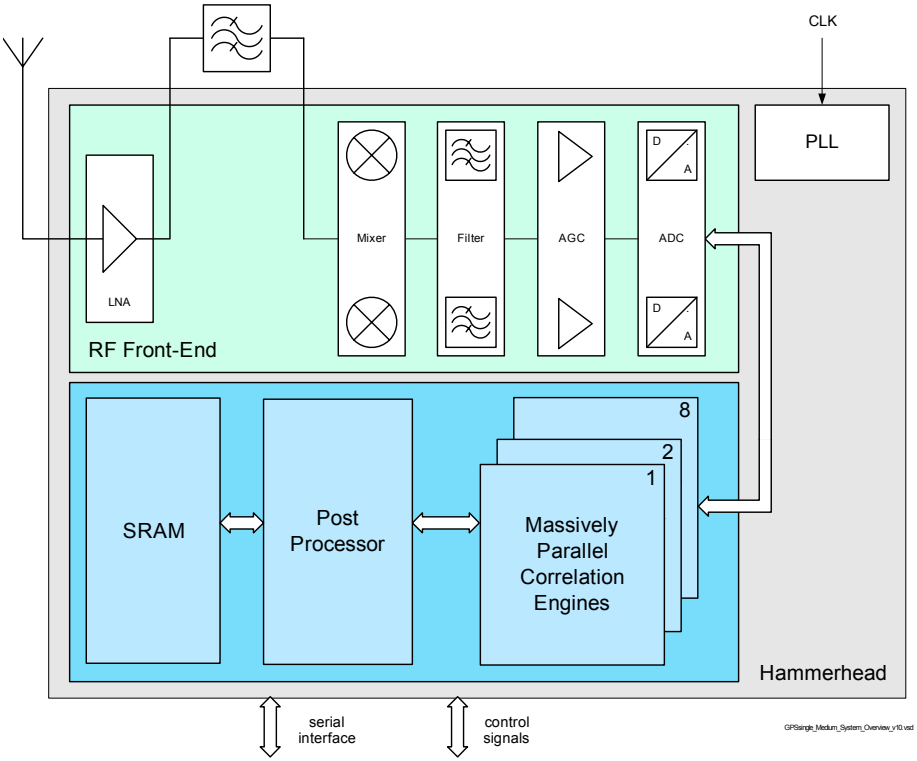
Figure 1-1 Hammerhead GPS Coarse System Architecture including Host CPU



A more detailed system diagram showing the modules integrated in the Hammerhead as well as an external SAW (surface acoustic wave) filter is shown in **Figure 1-2**. The Hammerhead consists of the following modules:

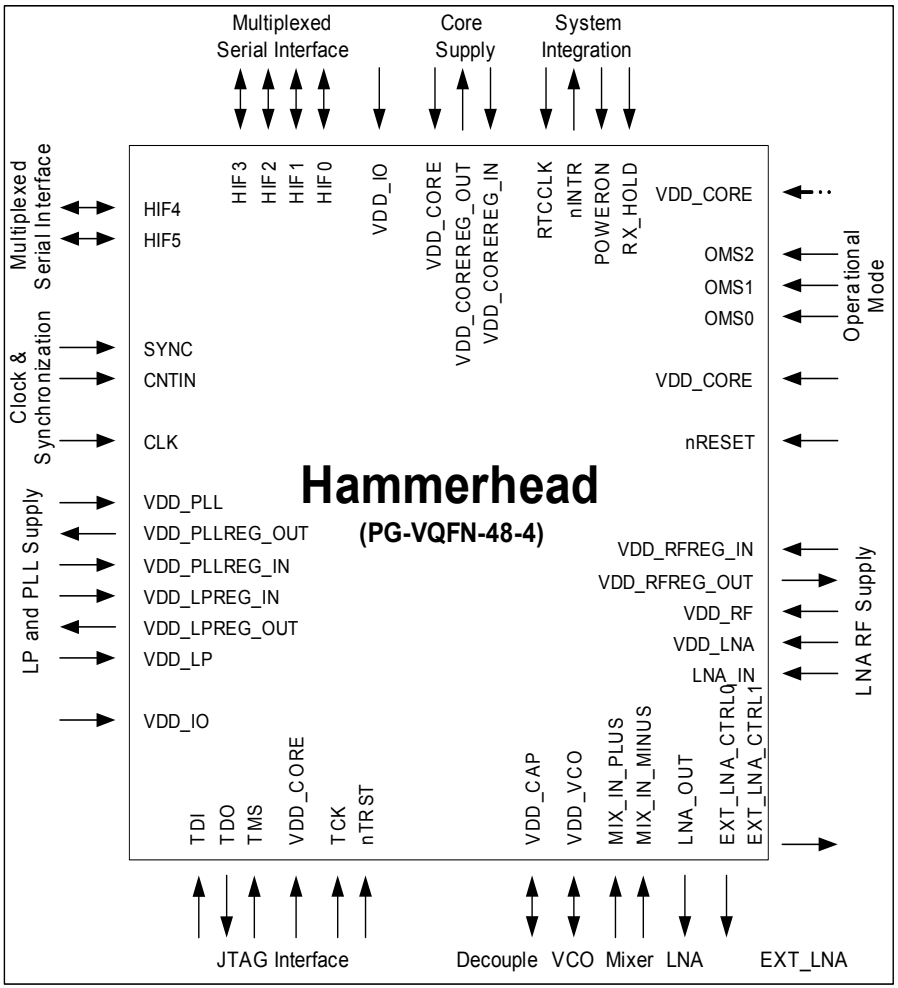
- RF front-end with on-chip, high gain and low noise, LNA, I/Q mixers, on-chip polyphase complex IF filter, digitally controlled AGC, and 3-bit ADC for the I and Q paths
- Sigma-Delta RF PLL with on-chip VCO and on-chip loop filter
- Embedded PLL and NCO for baseband clock generation
- 8 channels digital mixers and massive parallel correlator engines to enable real time correlation of the PRN code
- Post processor including peak detection logic
- SRAM for storing correlation results

Figure 1-2 Hammerhead Block Diagram Showing the Radio Receiver Frontend and the GPS Baseband Engine



1.3 Pin Configuration PG-VQFN-48-4

Figure 1-3 Logic Symbol of the Hammerhead (PG-VQFN-48-4) PMB 2520



GPSsingle_logic_symbol_vqfn_external_v10.vsd

1.4 Pin Description List (PG-VQFN-48-4)

Table 1-5 Pin List of Hammerhead (PG-VQFN-48-4)

Pin No.	Pin Name	Pad Type	Pad Usage		O/P State		
			Direction	Additional	Reset	Standby	Pad Functional Description
1	TDI	I/O	I	PU “C”	1	1	Serial Data Input (JTAG, IEEE 1149.1)
2	TDO	I/O	O	-	Z	Z	Serial Data Output (JTAG, IEEE 1149.1)
3	TMS	I/O	I	PU “C”	1	1	State Machine Control Signal (JTAG, IEEE 1149.1)
4	VDD_CORE	PI	-	-	-	-	Digital core supply
5	TCK	I/O	I	PD “C”	0	0	Clock (JTAG, IEEE 1149.1)
6	nTRST	I/O	I	PD “A”	0	0	Reset Input (JTAG, IEEE 1149.1)
7	VDD_CAP	AI/O	AI/O	-	(Z)	(Z)	RF Digital Supply Decoupling
8	VDD_VCO	AI/O	AI/O	-	(Z)	(Z)	Buffer capacitor for VCO supply
9	MIX_IN_PLUS	AI	AI	-	-	-	Differential mixer input
10	MIX_IN_MINUS	AI	AI	-	-	-	Differential mixer input
11	LNA_OUT	AO	AO	-	-	-	LNA output signal
12	EXT_LNA_CTRL0	AI/O	O	-	-	-	External LNA control
13	EXT_LNA_CTRL1	AI/O	O	-	-	-	External LNA control
14	LNA_IN	AI	AI	-	-	-	LNA input signal
15	VDD_LNA	PI	-	-	-	-	LNA supply voltage
16	VDD_RF	PI	-	-	-	-	IF RF circuit supply voltage
17	VDD_RFREG_OUT	PO	-	-	-	-	RF voltage regulator output
18	VDD_RFREG_IN	PI	-	-	-	-	RF voltage regulator input
19	nRESET	I/O	I	Hyst	0	1	Chip reset signal
20	VDD_CORE	PI	-	-	-	-	Digital core supply
21	OMS0	I/O	I	-	-	-	Operational mode select / Bus interface select
22	OMS1	I/O	I	-	-	-	Operational mode select / Bus interface select
23	OMS2	I/O	I	-	-	-	Operational mode select
24	VDD_CORE	PI	-	-	-	-	Digital core supply
25	RX_HOLD	I/O	I	-	-	-	RX_HOLD signal (From host to indicate that the host is transmitting)
26	POWERON	I/O	I	-	0	0	Power On signal to chip
27	nINTR	I/O	O	OD	Z	Z	Interrupt request signal to host
28	RTCCLK	I/O	I	Hyst	-	-	32.768kHz clock signal input
29	VDD_COREREG_IN	PI	-	-	-	-	Digital core voltage regulator supply

Table 1-5 Pin List of Hammerhead (PG-VQFN-48-4) (cont'd)

Pin No.	Pin Name	Pad Type	Pad Usage		O/P State		Pad Functional Description
			Direction	Additional	Reset	Standby	
30	VDD_COREREG_ OUT	PO	-	-	-	-	Digital core voltage regulator output
31	VDD_CORE	PI	-	-	-	-	Digital core supply
32	VDD_IO	PI	-	-	-	-	Digital I/O supply
33	HIF0 - / - / I²C_SCL / -	I/O	I I I²C I I	- - - - -	- - - - -	- - - - -	Host Interface OMS[2:0]=[1,1,1]: not used (tie to "0") OMS[2:0]=[1,1,0]: not used (tie to "0") OMS[2:0]=[1,0,1]: I²C clock OMS[2:0]=[1,0,0]: not used (tie to "0")
	-		-	-	-	-	OMS[2:0]=[0,x,x]: Reserved, Do not use.
34	HIF1 - / - / I²C_SDA / -	I/O	I I I²C I/O I	- - OD -	- - Z -	- - Z -	Host Interface OMS[2:0]=[1,1,1]: not used (tie to "0") OMS[2:0]=[1,1,0]: not used (tie to "0") OMS[2:0]=[1,0,1]: I²C data OMS[2:0]=[1,0,0]: not used (tie to "0")
	-		-	-	-	-	OMS[2:0]=[0,x,x]: Reserved, Do not use.
35	HIF2 UART_TXD / UART_TXD / I²C_GROUP0 / SPI_SCK	I/O	O Z I I	- - - -	0 Z - -	0 Z - -	Host Interface OMS[2:0]=[1,1,1]: UART Interface: Data Output OMS[2:0]=[1,1,0]: UART Interface: Data Output (Tristated) OMS[2:0]=[1,0,1]: Selection of I²C group address OMS[2:0]=[1,0,0]: SPI clock
	-		-	-	-	-	OMS[2:0]=[0,x,x]: Reserved, Do not use.
36	HIF3 UART_RXD / UART_RXD / I²C_GROUP1 / SPI_nSCS	I/O	I (I) I I	- - - -	- - - -	- - - -	Host Interface OMS[2:0]=[1,1,1]: UART Interface: Data Input OMS[2:0]=[1,1,0]: UART Interface: Data Input (Ignored) OMS[2:0]=[1,0,1]: Selection of I²C group address OMS[2:0]=[1,0,0]: SPI chip select
	-		-	-	-	-	OMS[2:0]=[0,x,x]: Reserved, Do not use.
37	HIF4 UART_nRTS / UART_nRTS / I²C_A0 / SPI_SI	I/O	O Z I I	- - - -	0 Z - -	0 Z - -	Host Interface OMS[2:0]=[1,1,1]: UART Interface: hardware flow control OMS[2:0]=[1,1,0]: UART Interface: hardware flow control (Tristated) OMS[2:0]=[1,0,1]: Selection of I²C group address bit 0 OMS[2:0]=[1,0,0]: SPI serial data input
	-		-	-	-	-	OMS[2:0]=[0,x,x]: Reserved, Do not use.
38	HIF5 UART_nCTS / UART_nCTS / - / SPI_SO	I/O	- I (I) I O/Z	- - - - -	- - - - Z	- - - - Z	Host Interface OMS[2:0]=[1,1,1]: UART Interface: hardware flow control OMS[2:0]=[1,1,0]: UART Interface: hardware flow control (Ignored) OMS[2:0]=[1,0,1]: not used (tie to "0") OMS[2:0]=[1,0,0]: SPI serial data output
	-		-	-	-	-	OMS[2:0]=[0,x,x]: Reserved, Do not use.

Table 1-5 Pin List of Hammerhead (PG-VQFN-48-4) (cont'd)

Pin No.	Pin Name	Pad Type	Pad Usage		O/P State		
			Direction	Additional	Reset	Standby	Pad Functional Description
39	SYNC	I	I	-	-	-	Digital reference time pulse
40	CNTIN	I	I	-	-	-	Digital high accuracy frequency reference
41	CLK	I/AI	I	-	-	-	Clock signal input. Selectable as digital or analog input
42	VDD_PLL	PI	-	-	-	-	Digital PLL supply
43	VDD_PLLREG_OUT	PO	-	-	-	-	PLL voltage regulator output
44	VDD_PLLREG_IN	PI	-	-	-	-	PLL voltage regulator input
45	VDD_LPREG_IN	PI	-	-	-	-	Low Power core regulator input
46	VDD_LPREG_OUT	PO	-	-	-	-	Low Power core regulator output
47	VDD_LP	PI	-	-	-	-	Low Power supply
48	VDD_IO	PI	-	-	-	-	Digital I/O supply
(49)	VSS	GND	-	-	-	-	Ground Pad. This is the exposed pad of the package

Table 1-6 Key to Table 1-5

Pad Type	Description	Comments
GND	Chip Ground	All signals are referred to this
PI	Power In	Supply to a voltage domain
PO	Power Out	Regulator Output
I/O	Digital Signal Pad	All Digital Pads are I/O Pads which are configured internally as required. - All are configured as Push-Pull except those marked as OD (open drain) - All have hysteresis by default, but is only mentioned when it is required for correct system operation.
AI	Analog Input	
AO	Analog Output	
PU	Internal Pull Up	See **Table 5-5** for definition of drive strengths "A" and "C".
PD	Internal Pull Down	See **Table 5-5** for definition of drive strengths "A" and "C".

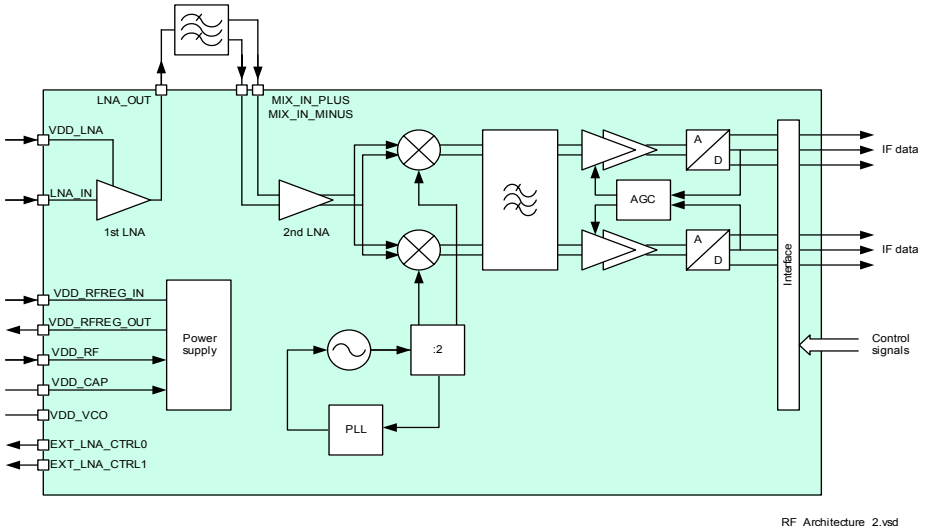
1.5 System Overview

1.5.1 RF frontend

The RF front-end integrates the following components:

- On-chip LNA
- I/Q mixers with pre-amplifier
- Polyphase complex IF filter
- Digitally controlled AGC with power level detection
- 3-bit A/D converters for I and Q paths
- Local Oscillator and PLL
- Voltage regulator

Figure 1-4 RF frontend block overview



1.5.1.1 On-chip LNA

The on-chip LNA is optimized to achieve high gain accompanied by a low noise figure and acceptable blocking performance.

1.5.1.2 I/Q mixers with pre-amplifier

The pre-amplifier has differential inputs, and the LNA gain is selectable. The mixers convert the RF to an IF signal.

1.5.1.3 Polyphase complex filter

The polyphase complex filter contains a low noise amplifier and a complex IF filter.

1.5.1.4 Digitally controlled AGC with power level detection

Following the complex bandpass filter an AGC, containing digitally controlled PGC IF amplifiers and a gain adjustment loop, will adjust the signal to a level suitable for the A to D converters. The PGC gain adjustment range is designed to handle a maximum of 16dB added external gain in addition to the 1st LNA.

1.5.1.5 3-bit A/D converters for I and Q paths

The AD converters digitize the I and Q signals for the baseband processing.

1.5.1.6 Local oscillator and PLL

The local oscillator and PLL generate the 0° and 90° phase shifted signals for the I-/Q-mixers. The VCO contains an automatic VCO trim procedure to trim the frequency to the intended one using the RF_CLK as reference.

1.5.1.7 Voltage regulator

The RF frontend contains a voltage regulator optimized to supply the RF frontend and the LNA.

1.5.1.8 Baseband interface

The RF front-end interfaces to the baseband subsystem via a tailored BB/RF interface and several control and configuration registers which control the operation of the RF front-end.

1.5.2 GPS Baseband

The GPS baseband implements a 8 channel digital GPS receiver each integrating the following components:

- Complex digital 4-quadrant mixer with a numerically controlled oscillator (NCO) signal generation
- Correlator processor with parallel correlator engines, PRN code generation and post correlation processor
- Correlation results SRAM with peak detection logic

The serial host interface can be configured, using the OMS pins, to one of the following interface types.

- UART
- I²C
- SPI

A clock PLL in the baseband generates the required internal clock signals from an external reference clock. Additionally a 32.768kHz clock signal is required. This 32.768kHz is also used for specific low-power modes.

1.5.3 Host software

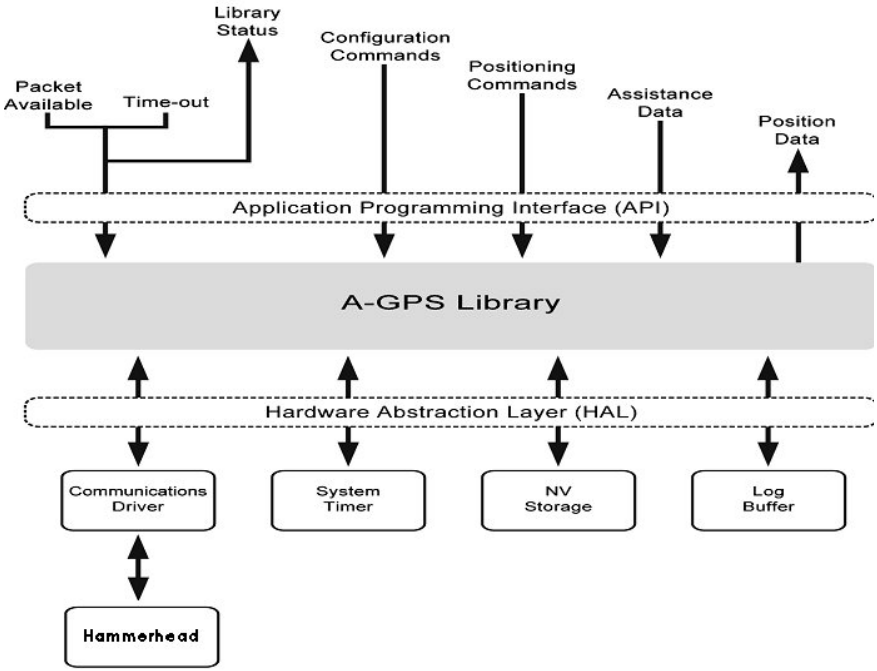
The Hammerhead system described in **Figure 1-1**shows the whole system including the mandatory software on the host. This software is required to configure and control the hammerhead chip, i.e. it is the software driver.

The host software is supplied with the hammerhead chip and is easily integrated on the host.

1.5.3.1 Host software Architecture

The Hammerhead driver software is delivered as a library specifically configured for the customer needs. The library has two dedicated interfaces for the host application software, see **Figure 1-5**. The “upper” part is the API that contains functionality used by the GPS navigation software presenting the location to the user. The “lower” API is the HAL (Hardware Abstraction Layer), interfacing the host system resources such as OS functions. The HAL needs to be adapted to the hardware and OS used in the host system.

Figure 1-5 Software Architecture



1.5.4 Test interface

A JTAG interface is integrated for test purposes and to allow boundary scan.

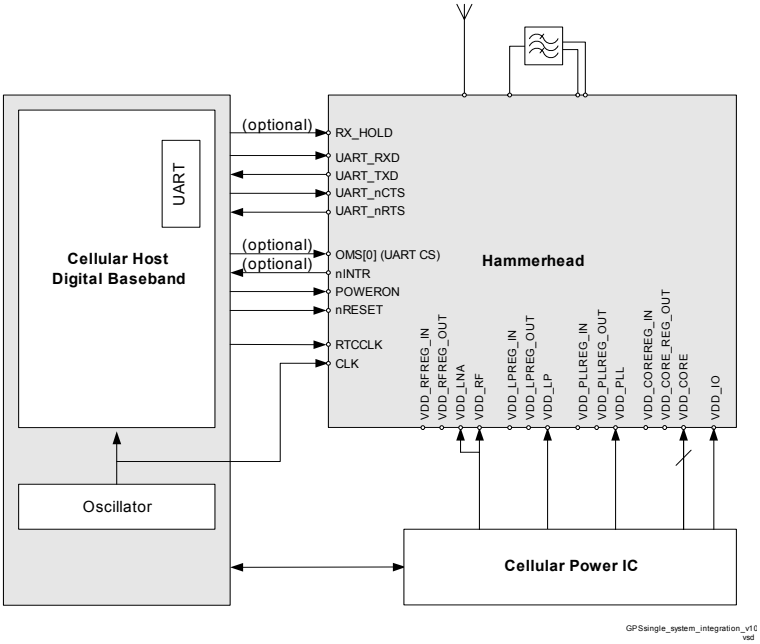
1.6 System Integration

In **Figure 1-6**, **Figure 1-7**, **Figure 1-8** and **Figure 1-9** the integration of the PMB 2520 Hammerhead A-GPS IC into a cellular host system is shown. **Figure 1-6** shows a system configuration in which the reference clock is provided by the cellular host system. The RF and digital voltages are supplied from the system power supply device using neither the internal RF voltage regulator, the VDD_Core voltage regulator, the PLL voltage regulator nor the Low Power voltage regulator.

A reference clock is provided by the host system. Additionally a 32.768kHz clock signal (RTCCLK) is required. This 32.768kHz is also used for specific low-power modes.

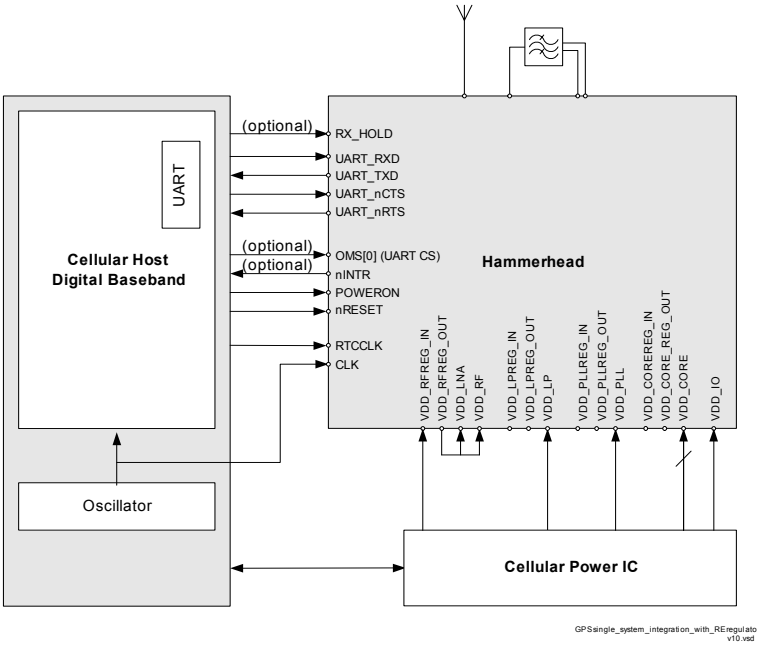
To switch the Hammerhead into and out of low-power modes the signal POWERON is provided.

Figure 1-6 Hammerhead Integration into a Host System connected by a Serial Interface without using any of the internal voltage regulators. (Example shows the UART as the serial interface).



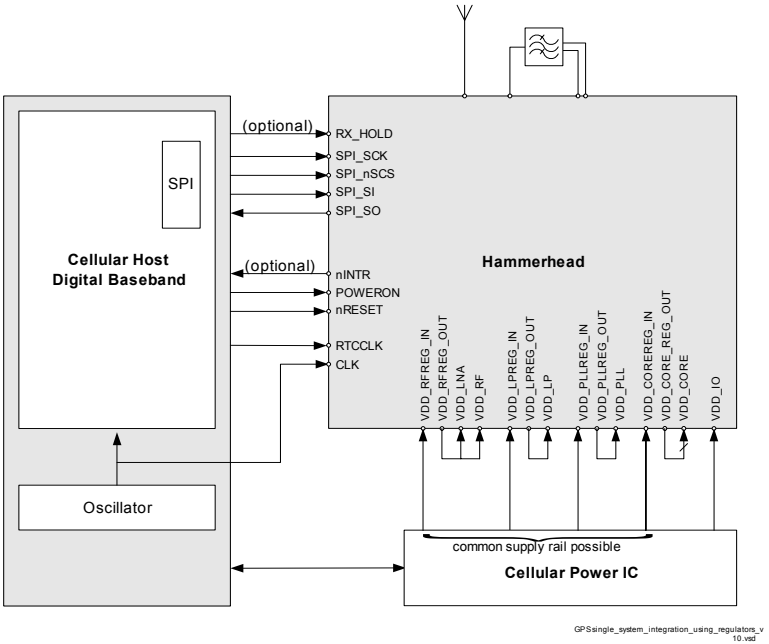
In **Figure 1-7** a system configuration is shown similar to the one in **Figure 1-6** but with the internal RF voltage regulator used.

Figure 1-7 Hammerhead Integration into a Host System connected by a Serial Interface using the internal RF voltage regulator. (Example shows the UART as the serial interface).



In **Figure 1-8** a system configuration is shown in which all the internal voltage regulators and the SPI interface is used.

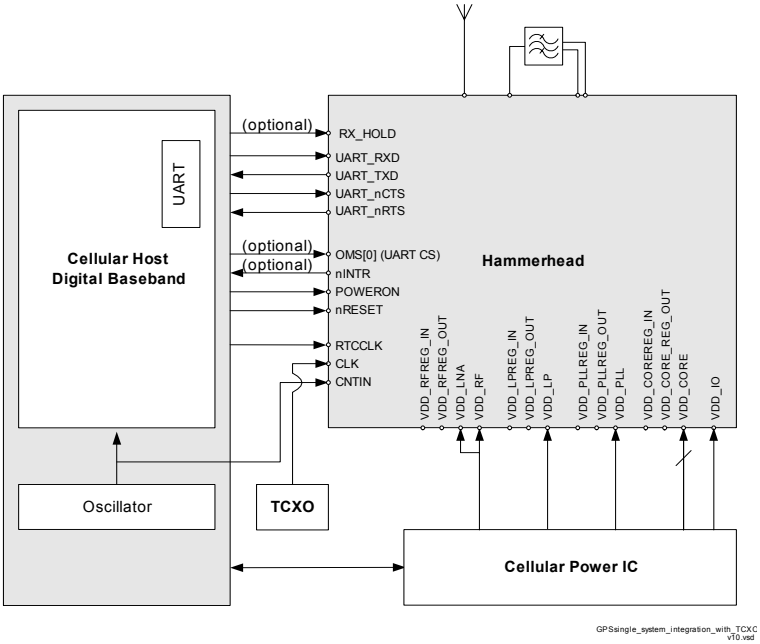
Figure 1-8 Hammerhead Integration into a Host System connected by a Serial Interface using all the internal voltage regulators. (Example shows the SPI as the serial interface).



In **Figure 1-9** a system configuration is shown in which the reference clock is provided by an external temperature-controlled crystal oscillator.

With the help of the signal CNTIN the cellular clock may be provided by the cellular system for calibration and synchronization purposes.

Figure 1-9 Hammerhead Integration into a Host System connected by a Serial Interface with external TCXO and additional Frequency Reference provided by the Cellular Host and without using the internal voltage regulators.
(Example shows the UART as the serial interface).



2 Host Interfaces

The Hammerhead integrates 3 serial interfaces:

- UART - Universal Asynchronous Receiver / Transmitter
- I²C bus - Inter-IC bus
- SPI - Serial Peripheral Interface

Since only one interface can be active in any specific system integration scenario, the interface signals are multiplexed onto the same pins. The exception being the I²C_SCL and I²C_SDA signals which are kept separate as the I²C switching levels on these pins are different. See **Table 1-5** for the pin list. Which interface is used in any particular application is selected by the OMS[2:0] pins according to the following **Table 2-1**.

Table 2-1 Host Interface Selection by OMS[2:0]

Host Interface	UART	UART(Disabled)	I²C	SPI
OMS[2]	1	1	1	1
OMS[1]	1	1	0	0
OMS[0]	1	0	1	0

In the following sections the interfaces together with the relevant status, control and data registers are described.

Note: As the UART INTERFACE may be bussed, the state OMS[110] disables the UART interface and puts the UART outputs from the Hammerhead (UART_TXD and UART_nRTS) *into tri-state mode. See **Chapter 2.1.6***

2.1 UART Host Interface

The Hammerhead provides a full-duplex UART (Universal Asynchronous Receiver Transmitter) interface which can be used to interface to an external host. The UART interface comprises the following features:

- Contains an NCO-based baud rate generator that enables generation of any baud rate from 1/4095th up to 1/32nd of the supplied reference clock frequency, and allows more flexibility than a simple integer divider.
- Automatic baud rate matching after reset.
- Programmable transmit pacing allows the Hammerhead UART transmit rate to be reduced without reducing the baud rate. This is achieved by inserting a configurable number of idle bits between transmitted characters, see **Table 2-2**. This reduced transfer rate relaxes the demands on the host UART receive path without impeding the host UART transmit rate.
- Supports hardware flow control through the use of nCTS (clear to send) and nRTS (ready for receiving) pins.
- 18-byte receiver FIFO enables the Hammerhead UART to be connected to an external UART without hardware flow control. (Software on the external host would implement flow control using GPIOs-the large receive FIFO allows the external UART to enable its up to 16-byte transmitter FIFO without causing an overrun in the Hammerhead.)
- Fixed 8N1 operation (8 data bits, no parity, 1 stop bit)
- False start bit, framing error, and overrun detection.
- Supports bussed UART mode via a chip select pin see **Chapter 2.1.6** and **Chapter 5.9.1**

2.1.1 Baud Rate Generator

After the Hammerhead is brought out of reset, the baud rate generator requires a series of synchronization (0x80) characters to be sent from the host to determine the baud rate. Bytes can be sent with either zero idle time or infinite idle time between them. This enables the Hammerhead to match the host's baud rate, and gives the host the flexibility to use any baud rate regardless of the reference clock frequency.

The baud rate generator provides the bit period clock, baud rate clock, to both the receiver and transmitter logic. The generated clock frequency is 16 times the baud rate to enable the receiver logic to perform accurate bit sampling.

2.1.2 Asynchronous Receiver

The UART_RXD pin is connected to a digital noise filter which removes short glitches up to 1/16th of the bit period from the received data signal.

The UART detects the start of a received character by sampling the UART_RXD pin until it receives a valid start bit. A valid start bit is defined as a low level (space) on the

UART_RXD pin which has a duration of at least 1/2 (8/16th) of the bit period. Spaces which are less than 1/2 of the bit period are ignored.

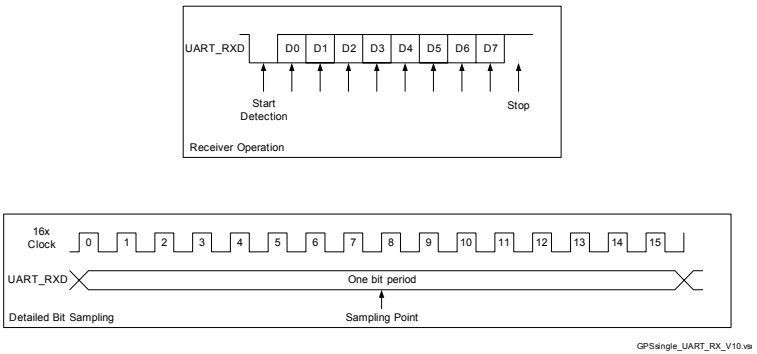
After a valid start bit is detected, the receiver samples at the assumed mid-point of every subsequent bit. (There will be up to 1/16th of a bit period initial phase error due to the 16X sampling clock rate, and a cumulative error which depends on the difference between the baud clock of the external transmitter and the Hammerhead receiver.)

If a character is received with an invalid stop bit (stop is sampled at a low level) then a framing error is generated. This information is provided to the UART interface. Note that if a break condition is present on UART_RXD pin, the Hammerhead will detect it as a framing error. If this occurs in the middle of a packet it will result in that packet being discarded, and if it occurs between packets the UART interface will ignore it.

After a character is received it is written to the receiver FIFO. If the receiver FIFO is full, then an overrun condition is recorded and made available to the UART interface. In normal operation the hardware flow control will prevent overruns from occurring.

The actual point at which UART_RXD is sampled is based on the 16X baud clock.

Figure 2-1 UART Reception

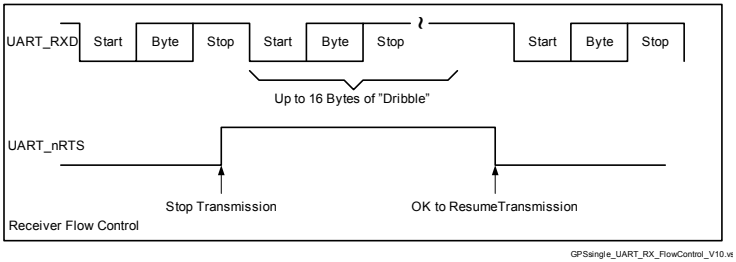


2.1.3 Receiver Flow Control

When the Hammerhead is ready to receive data, the UART_nRTS (ready for receiving) pin will be asserted low. The external host may send data to the Hammerhead whenever UART_nRTS is asserted, provided that the UART has been properly initialized. When the Hammerhead cannot keep up with the incoming data, it de-asserts the UART_nRTS pin by raising it to the high state. The external host is allowed to send up to 16 additional bytes after UART_nRTS is de-asserted. This is allowed because the external host may not recognize the de-assertion of UART_nRTS immediately, and may have loaded up to

16 bytes in its transmitter FIFO (the host's transmitter FIFO may not understand hardware flow control).

Figure 2-2 UART Receiver Flow Control



2.1.4 Asynchronous Transmitter

The transmitter transmits characters as they become available in the transmitter FIFO. The transmitter uses the 8N1 format which was previously shown for the asynchronous receiver. The transmitter can be disabled by the hardware flow control logic if the external host cannot keep up with the data rate.

2.1.5 Transmitter Flow Control

Before transmitting a character, the transmitter state machine checks the state of the UART_nCTS pin. When UART_nCTS is asserted (low) by the host, the Hammerhead UART transmitter will send out a character whenever one is available. When UART_nCTS is de-asserted by the external host, the Hammerhead will not transmit any characters (if UART_nCTS is de-asserted in the middle of a character transmission, the UART transmitter will complete the transmission of that character before idling). Depending on the timing of UART_nCTS versus the Hammerhead internal clocks, one additional character may be transmitted after UART_nCTS is de-asserted. As long as

UART_nCTS is de-asserted by the middle of the STOP bit, then no additional characters will be transmitted.

Figure 2-3 UART Transmitter Flow Control

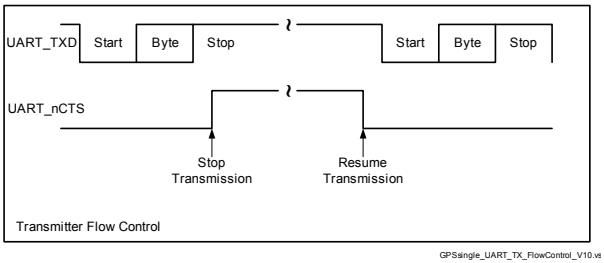


Table 2-2 Transmit pacing register

Register	Description
TX pacing[7:0]	UART transmit pacing - controls the number of idle bits inserted between transmitted characters. $\text{Effectivetxbaudrate} = \frac{10}{10 + \text{TXpacing}} \cdot \text{baudrate}$ Reset Value =8'h00

2.1.6 UART Chip Select

The UART interface is designed so that one host UART is able to communicate with multiple peripherals. This is achieved by the following:

- When OMS[2:0] is in the state [11x], i.e. the UART interface is being used then the OMS0 pin acts as an active high UARTCS. If the UART chip select feature is not needed, then this pin is coupled high.

When UARTCS is asserted high, then the UART behaves normally.

When UARTCS is de-asserted low, then the UART is not selected. The behaviour of the UART is modified as follows:

- TX - the TX line is tri-stated so that it may be shared with other UARTs.
- UART_nCTS - the UART_nCTS pin is ignored. It is treated as if it were de-asserted, so the UART transmitter will be disabled.

- UART_RX - the UART_RX line is ignored. Internally it is treated as if it were idle so that any serial activity directed to another UART will be ignored.
- UART_nRTS - the UART_nRTS line is tri-stated so that it may be shared with other UARTs.

2.2 SPI Host Interface

The SPI bus is a full duplex, synchronous interface.

The Hammerhead provides an industry standard SPI interface for use with hosts which contain a hardware SPI controller. It provides the following features:

- The maximum datarate is that the SPI interface supports is dependent on the reference clock, CLK, according to the formula: $(F_{CLK}/10)Mbps$, where F_{CLK} is the Reference clock frequency in MHz
- Support of SPI mode 0 (CPOL=0, CPHA=0)
- Support of normal SPI bit ordering (MSB first)
- Optional interrupt generation when the host needs to service the SPI slave.

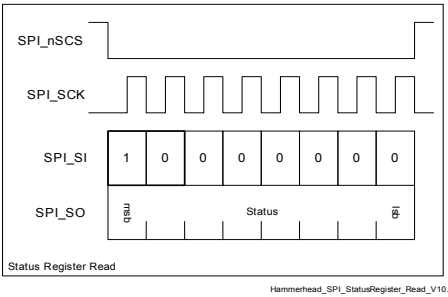
The Hammerhead only performs transfers that are a multiple of 8 bits.

For a description of the SPI timing see **Chapter 5.9.3**

2.2.1 SPI Cycles

The four supported transfer types are shown in the following four figures using a simplified notation.

Figure 2-4 SPI Status Register (Read)



Note: The status register read is shown for completeness. Because all of the operations begin with a status register read, it is not expected that a status register read will be performed as an isolated SPI bus event.

Figure 2-5 SPI Transmit Data Register (Reads)

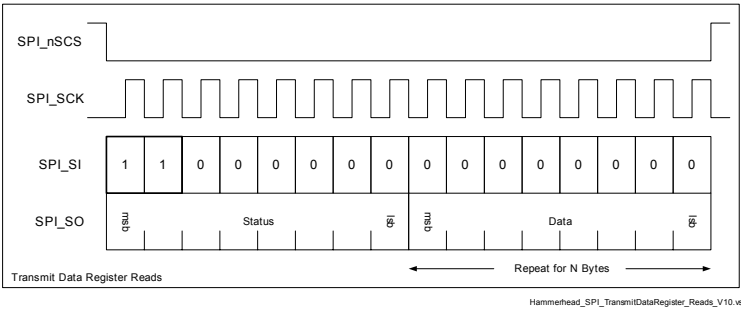


Figure 2-6 SPI Control Register (Write)

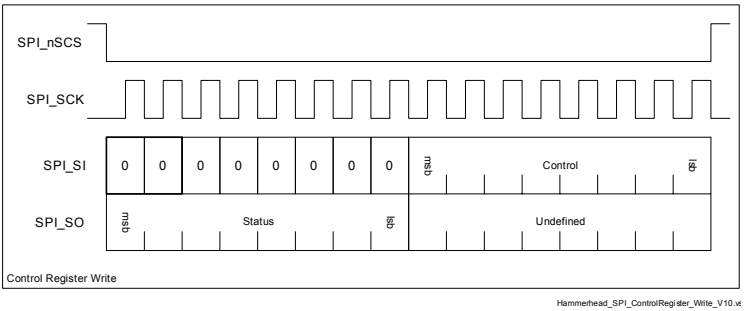
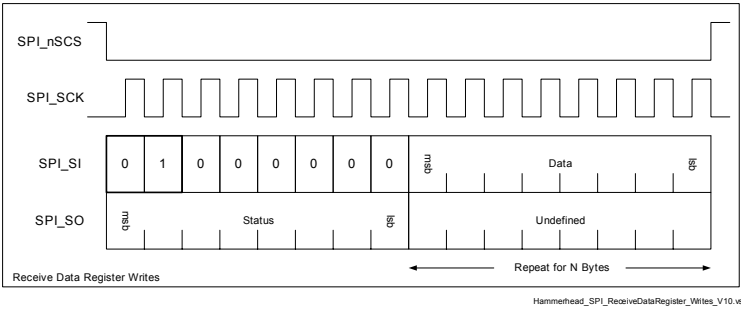


Figure 2-7 SPI Receive Data Register (Writes)



2.3 I²C Host Interface

The I²C interface comprises the following features:

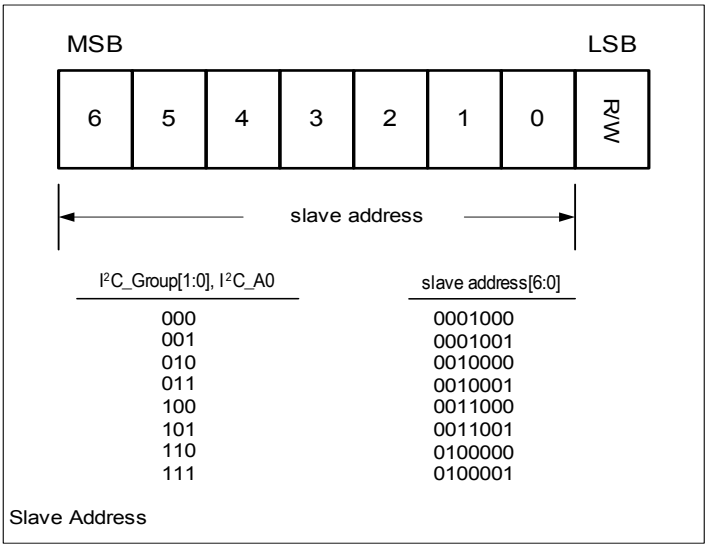
- Slave-only operation (slave transmitter and slave receiver).
- 7-bit device address.
- Supports standard (up to 100 kbit/s) and fast (up to 400 kbit/s) modes.
- Optional interrupt generation when the host needs to service the I²C slave.
- Slave never stretches the I²C_SCL low period.

For the I²C timing see **Chapter 5.9.2**.

2.3.1 I²C Slave Address

The Hammerhead slave address is determined by the state of the I²C_GROUP[1:0] and I²C_A0 pins. The Hammerhead will ignore any address except for its assigned slave address. Addresses outside of this range, including the general call address, START byte, CBUS address, reserved addresses, Hs-mode master code, and 10-bit slave addressing are ignored.

Figure 2-8 I²C Slave Address



2.3.2 I²C Read/Write Cycles

The four supported transfer types are shown in the following four figures.

Figure 2-9 I²C Status Register (Read)

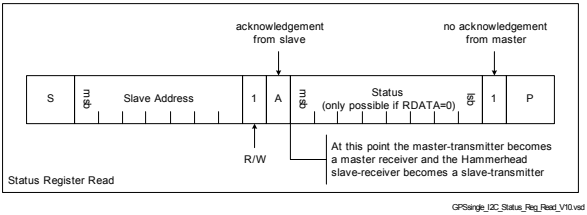
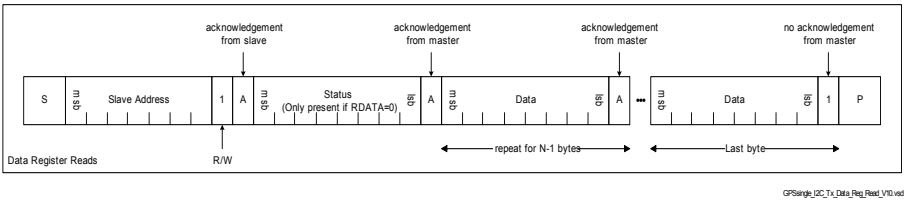


Figure 2-10 I²C Transmit Data Register (Reads)



*Note: Note that the data register reads are only preceded by a status register read if the RDATA control bit is cleared to zero, see **Figure 2-13**. Normally RDATA should be left cleared to zero as this behaviour is useful since software makes use of the*

status register read to determine how much data is available. Set RDATA to one only when required for operation with certain limited I2C masters.

Figure 2-11 I²C Control Register (Write)

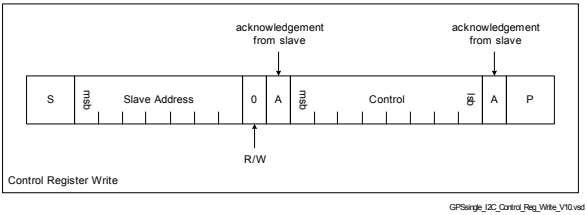
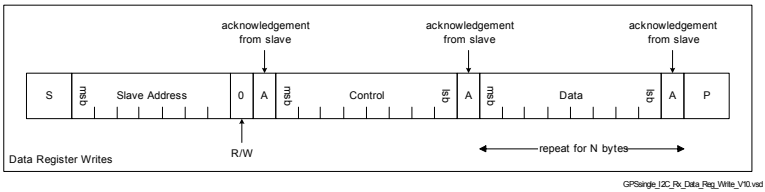


Figure 2-12 I²C Receive Data Register (Writes)



2.4 Status, Control, and Data Registers

The SPI and I²C serial interfaces contain status, control, and data registers which are used to send and receive data to the Hammerhead. The software is responsible for

avoiding data underruns and overruns. This is done by monitoring the REMPTY and TCNT fields in the status register.

Figure 2-13 Hammerhead Control Register (Write)

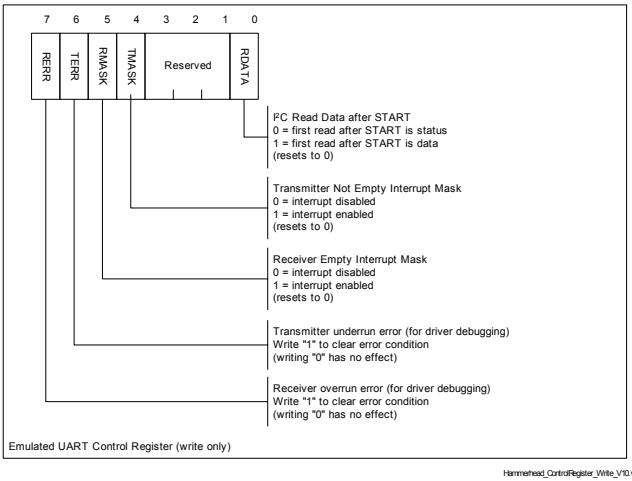


Figure 2-14 Hammerhead Status Register (Read)

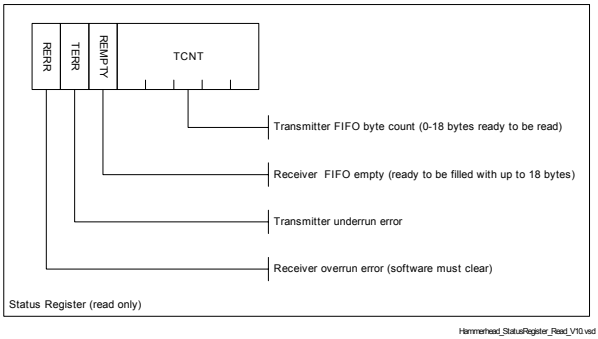


Figure 2-15 Hammerhead Receive Data Register (Write)

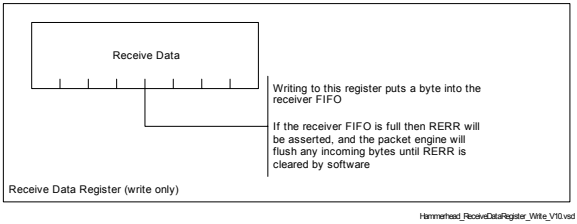
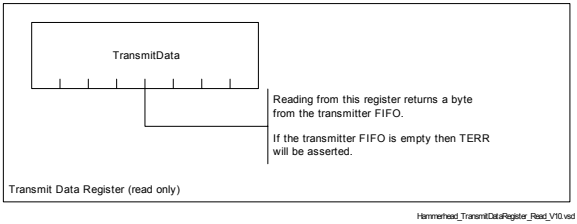


Figure 2-16 Hammerhead Transmit Data Register (Read)



2.5 nINTR

2.5.1 I²C and SPI

For the I²C and SPI interfaces the nINTR generation is controlled by the RMASK and TMASK in the control register. Software can use the TMASK (transmitter not empty interrupt mask) to detect when data is available to be read from the Hammerhead. This way software does not need to spend time polling the status register when the Hammerhead is active. The RMASK (receiver empty interrupt mask) bit can be used in the unlikely case that the Hammerhead isn't able to process data as fast as the host can transmit it.

2.5.2 UART

The nINTR signal allows the host to sleep during long integrations. Consequently it may not be able to receive serial data during this time. The Hammerhead uses this signal to wake-up the host before transmitting any data.

This is implemented as follows:

- The host transmits a packet to the Hammerhead telling it to enter SLEEP mode.
- The interrupt line nINTR will be asserted (low) whenever the UART is in SLEEP mode and there are characters in the UART transmit FIFO ready to be sent to the host.

- When the UART is in SLEEP mode then it will ignore any bytes transmitted by the host except for INTACK (interrupt acknowledge - 0xFA) and WAKE (0xFB). Also note that the host needs to leave nCTS asserted for the UART to be allowed to transmit any bytes. Therefore if nCTS is de-asserted when an INTACK byte is received, then the INTACK byte is ignored since its processing requires an interrupt status byte to be transmitted.
- When an INTACK byte is received and nCTS is asserted low, then the UART will transmit the interrupt status (0x7A = interrupt not asserted, 0x7B = interrupt asserted) and exit sleep mode only if the interrupt is currently asserted. (This behaviour facilitates sharing the interrupt with other peripherals.)
- When a WAKE byte is received, then the UART will exit sleep mode and will not transmit the interrupt status byte. This feature can be used to get the UART out of SLEEP mode.

The reason for not transmitting the interrupt status in response to receiving the WAKE byte is that this makes the software design easier in a system which uses a dedicated interrupt pin for the Hammerhead. Since the software is then able to acknowledge all interrupts with WAKE, knowing that all the interrupts are coming from the Hammerhead, without needing to check the interrupt status, this simplifies the UART receiver code - every incoming byte is a data byte.

When the UART is in SLEEP mode, it will not transmit any bytes unless instructed to do so by the host.

3 System Clocks description

3.1 Overview

The Hammerhead supports a wide variety of clock schemes. There are four clock interfaces of which two are mandatory, the Reference clock, CLK and RTCCLK

The RTCCLK is used to clock the standby timer in low power modes and thus is required for low power operation.

The SYNC signal input is used if GPS timing is already available in the system; this is used to develop a relationship between the GPS timing and the Reference clock (CLK) in the Hammerhead.

The CNTIN is an external high frequency reference clock input which can be derived from network timing in for instance GSM systems.

3.2 Reference clock

The Hammerhead makes use of an external reference clock signal, 10-40MHz, provided by the host system, as shown in **Figure 1-6**, or a standalone TCXO, as shown in **Figure 1-9**. The Internal ΣΔ Clock PLL is driven from this clock, and provides the master clock used for the correlator blocks. A wide range of reference clocks can be used, due to the PLLs flexible fractional-N divider. The reference clock is set, based on user-defined constants in the driver software on the host, and can be tailored to a specific system frequency plan.

The clock input contains an amplifier (ICA) to enable the use of an analog clock. The clock mode, analog or digital, is configureable by software.

3.2.1 UART, SPI and I2C interfaces

The UART, SPI and I^2C interfaces are not driven by the PLL. These interfaces use the external reference clock directly. This makes it possible for the software to power down or change settings of the PLL, while the interfaces still are accessible.

3.3 SYNC clock

The SYNC clock is used in systems which are synchronized to an external source of GPS time. In such designs, a precise digital synchronization signal (SYNC) is input to the chip so that this counter can measure the time difference between GPS timing and the internal clock. The measurement data is used by the navigation control software to establish a precise relationship between the Hammerhead internal clocks and the external time source.

3.4 CNTIN clock

The CNTIN clock provides a means for measuring the reference frequency (CLK) relative to a separate, high-accuracy external digital reference signal (CNTIN).

3.5 RTCCLK

The RTCCLK is a 32.768kHz digital clock. This clock can be used in Power Down Mode, see **Table 4-2**. The Hammerhead maintains GPS time by using the RTCLK when the CLK is unavailable and is mandatory for low power operations. RTCCLK is also used to exit reset.

4 Power Management

4.1 Power Supplies and Voltage Regulators

Power to the Hammerhead device can be supplied from:

- The internal voltage regulators
- External regulated voltage supplies
- A combination of the above

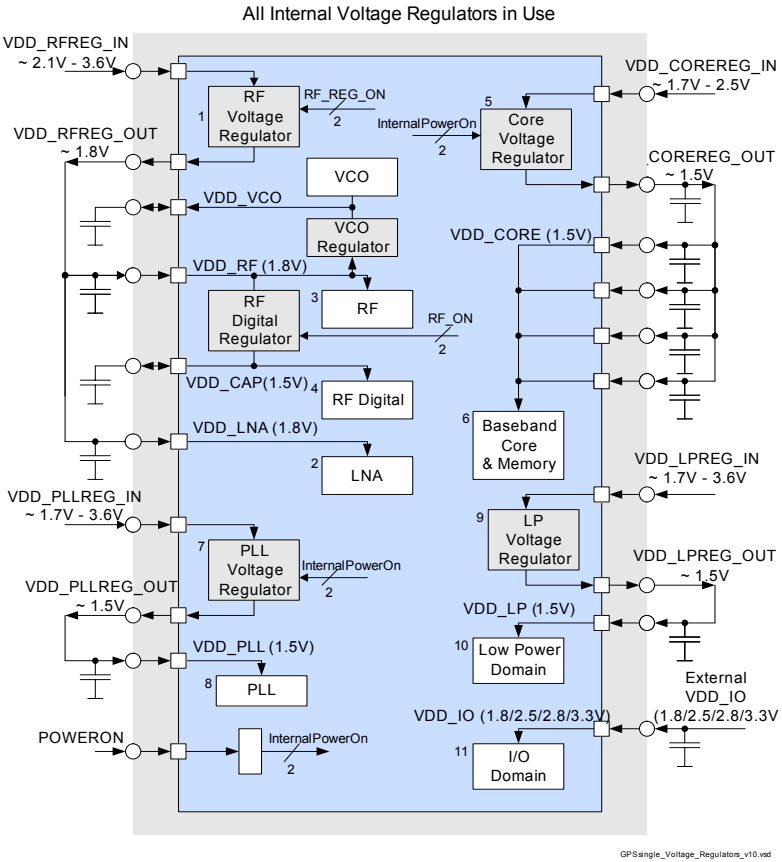
4.1.1 Internal voltage regulators.

If an internal voltage regulator is being used, the regulator output must be connected to the corresonding Vdd input. If the regulator is not used it is left unconnected.

See **Figure 4-1** for a complete illustration.

The internal regulators are controlled by the host software, except the LP voltage regulator which is always enabled.

Figure 4-1 Voltage regulators being used to supply the voltage domains.



See **Table 5-11** for decoupling values.

Note: The VDD_CAP and VDD_VCO pins are only available for decoupling purposes. No current should be forced in or extracted from these pins

4.1.2 External regulated voltage supplies.

The External Regulators must be switched on and off by the external host.

4.1.3 A combination of the above.

Any combination of internal and external regulators can be used depending on the supplies available in the host system.

4.2 Power Up and Power Down Sequencing

In order to avoid problems with ESD or outputs being forced into the wrong state(s) the following sequences should be adhered to when powering up or powering down the Hammerhead. See **Figure 4-2** or **Figure 4-3**

4.2.1 Power Up Sequence

The following sequence should be used for “Powering Up” the Hammerhead when using the nRESET:

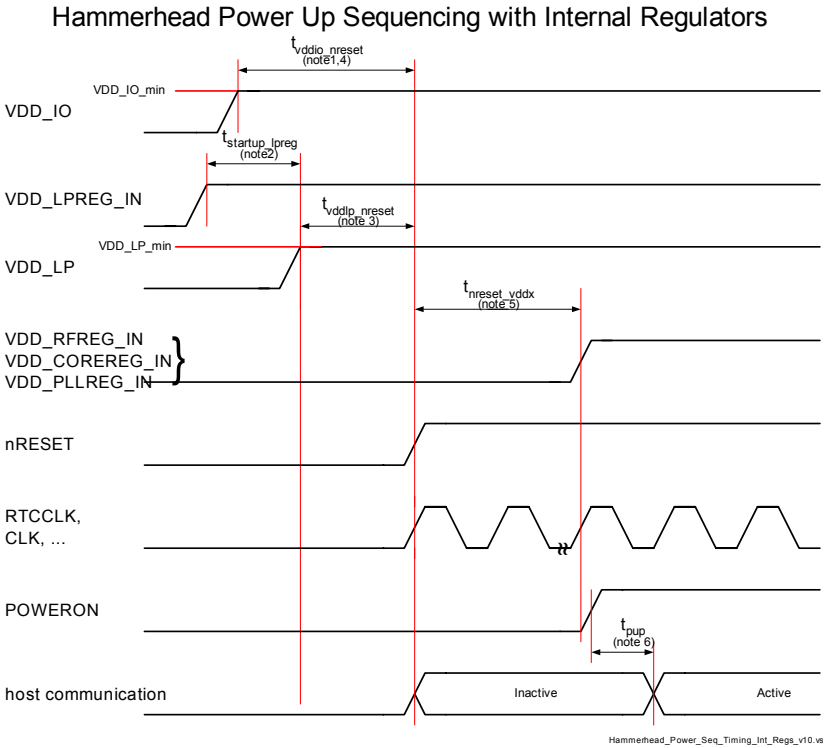
- Make sure no interfacing signals are driving current into the device.
  nRESET must be asserted (low) and
  POWERON must be de-asserted (low).
- Apply VDD_IO and VDD_LP, alternatively VDD_LPREG_IN.
- After VDD_IO has been stable for t_{vddio_nreset}, see **Table 4-1**, and VDD_LP has been stable for t_{vddlp_nreset}, see **Table 4-1**, de-assert nRESET (high).
  Hammerhead is now in Power Down Mode, according to **Table 4-2**.
- Apply VDD_CORE alternatively VDD_COREREG_IN, VDD_PLL alternatively VDD_PLLREG_IN and VDD_RFREG_IN alternatively VDD_RF
- Assert pin POWERON (high)
  This enables the CORE and PLL regulators (if used).
  Hammerhead is now in Software Only Standby.
- After 1 ms, the power supplies will be stable.
- After the reset sequence is complete the host can communicate through the serial interface.

4.2.2 Power Down Sequence

The following sequence should be used for “Powering Down” the Hammerhead:

- From Software Only Standby mode, de-assert the POWERON pin.
  This disables the CORE and PLL regulators (if used).
  The Hammerhead is now in Low Power Standby or Power Down Mode, see **Table 4-2**.
- Make sure no interfacing signals are driving current into the device.
- Remove VDD_CORE alternatively VDD_COREREG_IN, VDD_PLL alternatively VDD_PLLREG_IN and VDD_RFREG_IN alternatively VDD_RF
- Remove VDD_IO and VDD_LP alternatively VDD_LPREG_IN.
  The device is now completely powered off

Figure 4-2 Hammerhead Power Up Sequencing with Internal Regulators.



Note: 1: Delay from VDD_IO to nRESET or any digital input signal set high >= t_{vddio_nreset} to minimize current consumption during initial power sequencing.

Note: 2: VDD_LPREG_IN should be applied $t_{startup\_lpreg}$ before VDD_LP min is required.

Note: 3: nRESET must remain asserted for t_{vddlp_nreset} after VDD_LP is within limits to guarantee that the chip is set up correctly.

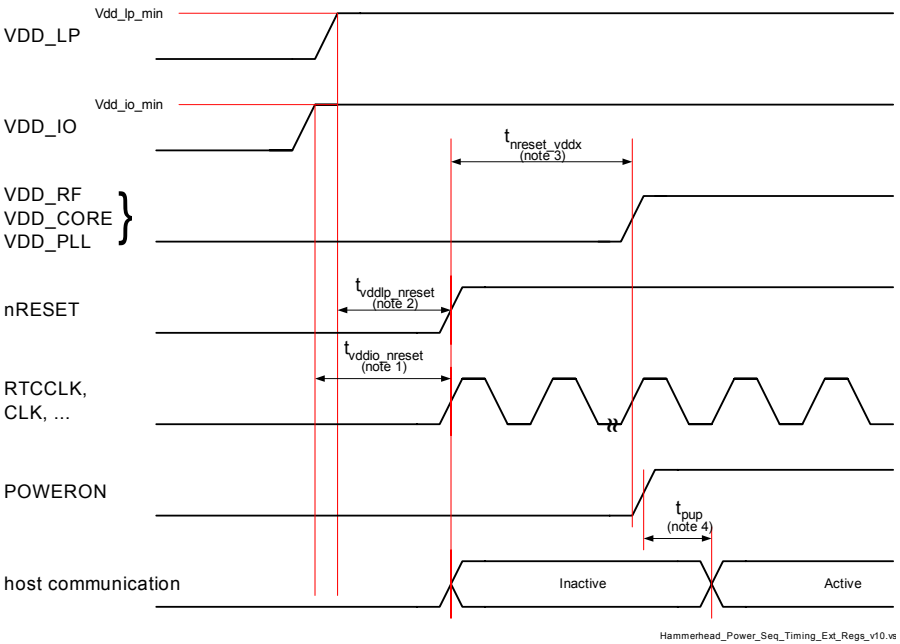
Note: 4: Delay from VDD_IO to any digital signal input high must be >=0 and should be greater than t_{vddio_nreset} to minimize current consumption during initial power sequencing.

Note: 5:t_{nreset_vddx} should be > 0 before POWERON is asserted.

Note: 6:Delay from POWERON to nReset_core de-asserted. Programmable from 1.9-15.6ms. Bus interface will not accept transfers until t_{pup} has been met. POWERON is controlled by software.

Figure 4-3 Hammerhead Power Up Sequencing with External Regulators.

Hammerhead Power Up Sequencing with External Regulators



Note: 1:Delay from VDD_IO to nRESET or any digital input signal set high >= t_{vddio_nreset} to minimize current consumption during initial power sequencing.

Note: 2:nRESET must remain asserted for t_{vddlp_nreset} after VDD_LP is within limits to guarantee proper chip initialization.

Note: 3:Delay from VDD_IO to any digital signal input high must be >=0 and should be greater than t_{pw_nreset} to minimize current consumption during initial power sequencing.

Note: 4:Delay from POWERON to nReset_core de-asserted.Programmable from 1.9-15.6ms. Bus interface will not accept transfers until t_{pup} has been met.
POWERON is controlled by software

Table 4-1 Power sequencing parameters

Parameter	Value	Comment
t_{vddio_nreset}	>500ns	This to ensure that no unnecessary current is drawn
$t_{startup\_lpreg}$	>1ms	See **Table 5-12 "Regulator Limits (Dynamic)" on Page 54**
t_{vddlp_nreset}	>50ns	Allowing the control signals to be settled to the IO pads
t_{nreset_vddx}	>500ns	This to ensure that no unnecessary current is drawn
t_{pup}	1.9-15.6ms	Programmable delay from POWERON until circuit fully functional.

4.3 Power Modes

The Hammerhead device supports three operational modes and three standby modes. These are defined in **Section 4.3.1** to **Section 4.3.6** below.

Table 4-2 Hammerhead operational modes

Mode	Conditions	Function	CLK	RTCLK	Control
Full Processing	All supply voltages and clocks are applied	This gives the peak performance with respect to TTFF. Core frequency normal	ON	ON	Software POWERON pin =1
Reduced Processing	All supply voltages and clocks are applied	This reduces the peak current required but also gives longer TTFF Core frequency reduced	ON	ON	
Software Only Standby	All supply voltages and clocks are applied	RF frontend off and Correlator clock off. Core frequency either normal or reduced	ON	ON	
Low Power Standby	Only VDD_LP and VDD_IO supplies are applied Reference clock on	No correlations active and core and PLL turned off. Time is kept with RTCCLK	OFF	ON	Software, POWERON pin =0
Power Down	Only VDD_LP and VDD_IO supplies are applied Reference clock off	No timekeeping. RTCCLK must be on to exit reset.	OFF	ON	
IC off	All supplies off	No activity and no data saved	OFF	OFF	

4.3.1 Full Processing Mode

The device is fully active.

- All supply voltages and clocks are applied.
- Correlators are running at 72 MHz. This is the mode that gives peak performance with respect to TTFF and energy usage.

4.3.2 Reduced Processing Mode

The device is fully active.

- All supply voltages and clocks are applied.
- Correlators are running at 48 MHz. This mode is used to reduce the peak current required by the VDD_CORE supply. It can be used if the system power supply device(s) have current limitations. The host software chooses this mode.

In both the above processing modes dynamic power saving occurs automatically. After a correlator has acquired sufficient data for a fix, the clocks to that correlator are internally disabled.

If no correlations are taking place, the hardware can automatically turn off parts of the RF block.

4.3.3 Software Only Standby

No correlations are taking place

- The RF Front-end is turned off, either by disabling the RF circuitry, disabling the RF voltage regulator, or externally switching the RF supply off. (Depending on Platform Application)
- The clocks to the correlators are turned off.

The rest of the device is fully active

4.3.4 Low Power Standby

No correlations are taking place and the core is turned off.

- Only the VDD_LP and the VDD_IO voltage supplies are applied.
- The Standby Counter is clocked with RTCCLK.

4.3.5 Power Down

No correlations are taking place and the core is turned off.

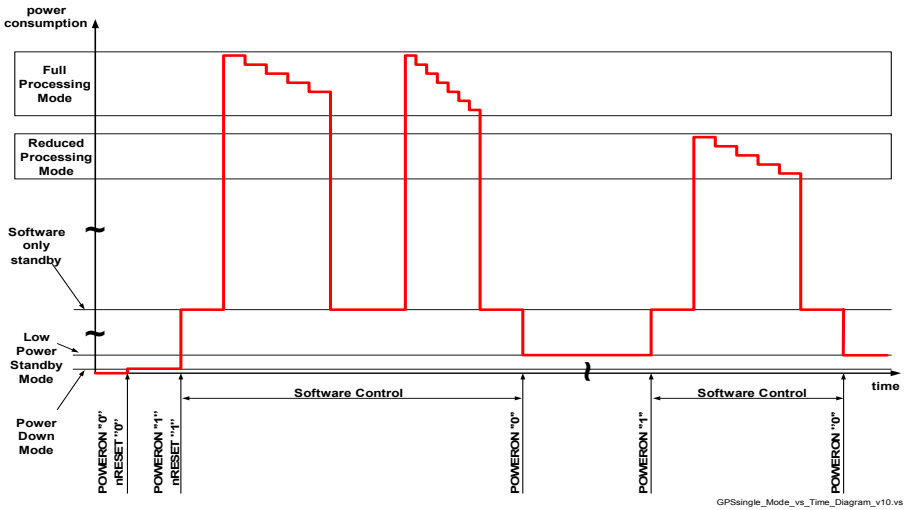
- Only the VDD_LP and the VDD_IO voltage supplies are applied.
- RTCCLK, 32.768 kHz, must be on to exit reset.
- No time keeping in Power Down mode

4.3.6 IC Off

- All supplies to the IC are off.
- No Voltages on any of the I/Os

If a bus architecture is being used on the platform, this mode cannot be used as signal voltages may be present on the interface inputs.

Figure 4-4 Operational Modes vs. Time (not to scale)



5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings.

Parameter	Limit Values		Unit	Notes
	min.	max.		
Storage temperature	-55	150	°C	
RF Regulator input voltage	-0.9	4.0	V	VDD_RFREG_IN
RF Regulator output voltage	-0.9	4.0	V	VDD_RFREG_OUT
RF Supply voltages	-0.9	4.0	V	VDD_LNA VDD_RF
Voltage on any RF pin	-0.9	4.0	V	
Core Regulator input voltage	-0.9	4.0	V	VDD_COREREG_IN
Core Regulator output voltage	-0.3	1.98	V	VDD_COREREG_OUT
Core Supply voltages	-0.3	1.98	V	VDD_CORE
Voltage on any Digital pin	-0.9	4.0	V	
Low Power Regulator input voltage	-0.9	4.0	V	VDD_LPREG_IN
Low Power Regulator output voltage	-0.3	1.98	V	VDD_LPREG_OUT
Low Power Supply voltages	-0.3	1.98	V	VDD_LP
Baseband PLL Regulator input voltage	-0.9	4.0	V	VDD_PLLREG_IN
Baseband PLL Regulator output voltage	-0.3	1.98	V	VDD_PLLREG_OUT
Baseband PLL Supply voltages	-0.3	1.98	V	VDD_PLL
I/O supply voltage	-0.9	4.0	V	VDD_IO
DC current on any Digital pin	-100	100	mA	

Note: Stresses above those listed here are likely to cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the integrated circuit.
Maximum ratings are not operating conditions.

5.2 Operating Ranges

Table 5-2 Operating Ranges (See Figure 5-1)

Parameter	Limit Values			Unit	Notes
	min.	typ.	max.		
Operating ambient temperature	-30	-	85	°C	
RF Regulator input voltage (1)	2.1	-	3.63	V	VDD_RFREG_IN
RF Regulator output voltage (3)	-	1.8	-	V	VDD_RFREG_OUT
RF Supply voltages	1.72	1.8	1.98	V	VDD_LNA VDD_RF
Voltage on any RF pin except LNA_IN, LNA_OUT	0	-	VDD_RF	V	
Voltage on LNA_IN, LNA_OUT	0	-	VDD_LNA	V	
Core Regulator input voltage (2)	1.7	-	2.5	V	VDD_COREREG_IN
Core Regulator output voltage (3)	-	1.5	-	V	VDD_COREREG_OUT
Core Supply voltages	1.41	1.5	1.6	V	VDD_CORE, Short transients(<150us) of up to +100mV outside max is acceptable
Low Power Regulator input voltage (2)	1.7	-	3.6	V	VDD_LPREG_IN
Low Power Regulator output voltage (3)	-	1.5	-	V	VDD_LPREG_OUT
Low Power Supply voltages	1.41	1.5	1.6	V	VDD_LP, Short transients(<150us) of up to +100mV outside max is acceptable
Baseband PLL Regulator input voltage (2)	1.7	-	3.6	V	VDD_PLLREG_IN
Baseband PLL Regulator output voltage (3)	-	1.5	-	V	VDD_PLLREG_OUT
Baseband PLL Supply voltages	1.41	1.5	1.6	V	VDD_PLL, Short transients(<150us) of up to +100mV outside max is acceptable
I/O supply voltage	1.62	-	3.63	V	VDD_IO
DC current on any Digital pin	-100	-	100	mA	

Note: (1) To minimize system power usage these regulators should be run from a 2.2V (+/-100mV) supply.

There is a maximum voltage drop across the regulators of 380mV for these conditions.
(2) *To minimize system power usage these regulators should be run from a 1.8V (+/-100mV) supply.*
There is a maximum voltage drop across the regulators of 290mV for these conditions.
(3) See ***Table 5-11*** *and* ***Table 5-12*** *for more details.*

5.3 DC Characteristics

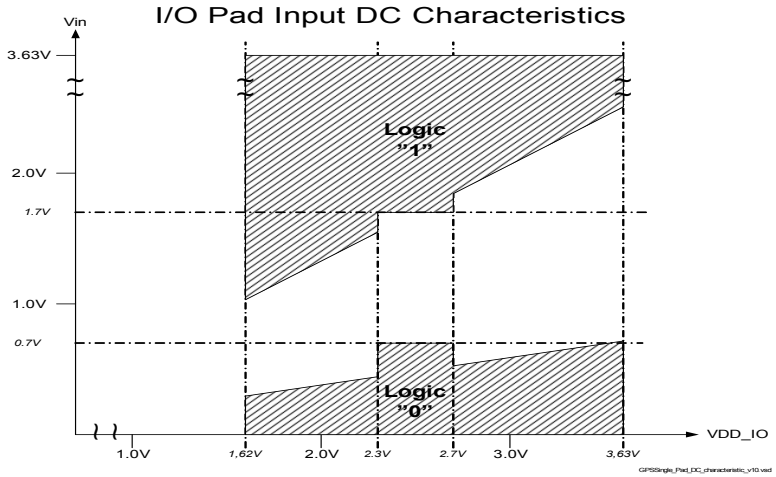
5.3.1 DC characteristic Digital I/O Pads

Table 5-3 DC characteristic Digital I/O Pads

Symbol	Parameter	Conditions	Limit Values		Unit
			min.	max.	
V_{IL}	Input low voltage	1.62V≤VDD_IO≤2.3V	-0.3	0.2 * VDD_IO	V
V_{IL}	Input low voltage	2.3V<VDD_IO≤2.7V	-0.3	0.7	V
V_{IL}	Input low voltage	2.7V<VDD_IO≤3.63V	-0.3	0.2 * VDD_IO	V
V_{IH}	Input high voltage	1.62V≤VDD_IO≤2.3V	0.7 * VDD_IO	VDD_IO+0.3	V
V_{IH}	Input high voltage	2.3V<VDD_IO≤2.7V	1.7	VDD_IO+0.3	V
V_{IH}	Input high voltage	2.7V<VDD_IO≤3.63V	0.7 * VDD_IO	VDD_IO+0.3	V
V_{OL}	Output low voltage	I_{OL}= 100µA	-	0.2	V
V_{OL}	Output low voltage	I_{OL}= 2mA	-	0.4	V
V_{OH}	Output high voltage	I_{OH}=-100µA	VDD_IO - 0.2	-	V
V_{OH}	Output high voltage	I_{OH}=-2mA	VDD_IO - 0.4	-	V
V_H	Hysteresis	RTCCLK(1) nRESET(1)	200m	-	V
C_{IN}	Capacitance		-	10p	F
I_L	Leakage Current	V_{PAD}=0 or VDD_IO	-	±2µ	A

Note: (1) All Digital I/O Pads have hysteresis.
However it is only these two that require hysteresis for correct system operation.

Figure 5-1 Digital I/O Pads Input DC Characteristics.



5.3.2 DC characteristic I²C Pads (I²C_SCL, I²C_SDA) .

Table 5-4 DC characteristic I²C Pads (I²C_SCL, I²C_ SDA)

Symbol	Parameter	Conditions	Limit Values		Unit
			min.	max.	
V_{IL}	Input low voltage	1.62V≤VDD_IO≤ 2.5V	-0.3	0.25 * VDD_IO	V
V_{IL}	Input low voltage	2.50V<VDD_IO≤ 3.63V	-0.3	0.3 * VDD_IO	V
V_{IH}	Input high voltage	-	0.7 * VDD_IO	VDD_IO+0.3	V
V_{OL}	Output low voltage	I_{OL}= 700µA	-	0.2	V
V_{OH}	Output high voltage	-	-	VDD_IO+0.3	V
C_{IN}	Input Capacitance	-	-	10p	F
I_L	Leakage Current	V_{PAD}=0 or VDD_IO	-	±2µ	A
t_{NS}	Pulse Width Ignored	1.62V≤VDD_IO≤ 2.5V	-	50n	s
t_{NS}	Pulse Width Ignored	2.50V<VDD_IO≤ 3.63V	-	35n	s

5.3.3 Pull-Up and Pull-Down Values of JTAG interface

Table 5-5 Pull-Up and Pull-Down Values of JTAG interface

Symbol	Pull Up			Pull Down			Unit	Notes
	min.	typ.	max.	min.	typ.	max.		
TMS	3.5	6.0	10.0	-	-	-	µA	Pull Up
TCK	-	-	-	2.3	4.9	9.1	µA	Pull Down
TDI	3.5	6.0	10.0	-	-	-	µA	Pull Up
TDO	-	-	-	-	-	-	µA	Output. High Z in functional mode
nTRST	-	-	-	72	145	260	µA	Pull Down

5.4 CLK Input Clock Amplifier (ICA) characteristics

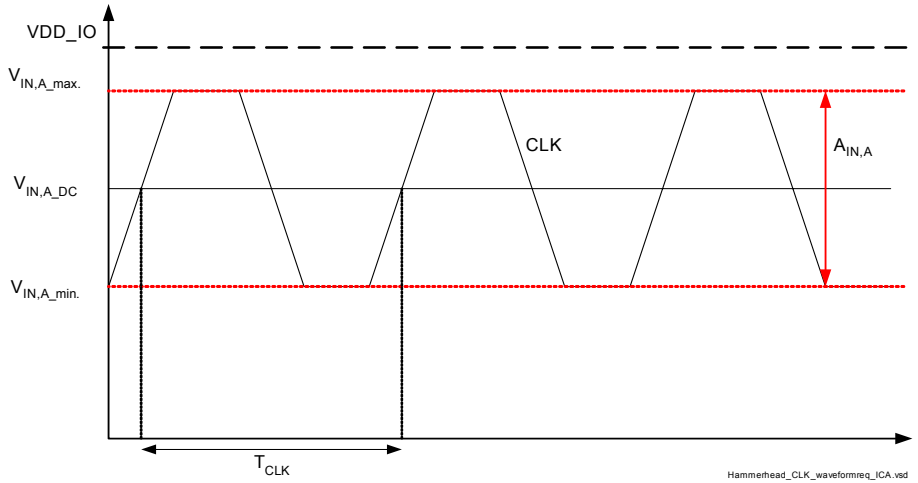
Table 5-6 Characteristics (ICA)

Symbol	Parameter	Cond.	Limit Values			Unit
	Analog mode		**min.**	**typ.**	**max.**	
$V_{IN,A}$	Input Voltage		0		VDD_IO	V
$A_{IN,A}$	Input Amplitude (Clipped sinus p-p)		0.2		VDD_LP	V
	Wave form requirement			Sine, clipped sine or square		
$R_{IN,A}$	Input Impedance			25k		Ω
$C_{IN,A}$	Input Capacitance			2.5p		F
f_{in}	Frequency input range(1)		10M		40M	Hz
	Square Duty cycle input		20%		80%	
I_A	Current Consumption(2)			20µ	195µ	A
$t_{startup}$	Startup time for the CLK pad(3)				2µ	s
	Digital mode		**min.**	**typ**	**max**	**Unit**
$V_{IL,D}$	Input low voltage		0	-	VDD_LP *0.3	V
$V_{IH,D}$	Input high voltage		VDD_LP *0.7	-	VDD_IO	V
f_{in}	Input frequency		0		40M	Hz
$R_{IN,D}$	Input Impedance			25k		Ω
$C_{IN,D}$	Input Capacitance			2.5p		F
T_{DC}	Square Duty Cycle at Input		20%		80%	
$I_{(in)}$	Input leakage current				1µ	A
$I_{(VDD)}$	Current Consumption (4)			5µ	78µ	A
$t_{startup}$	Startup time for the CLK pad(3)				2µ	s

Note: (1) Clock must be applied before the POWERON signal is asserted (high)
(2) Typical value very dependant on input clock signal. Lower f_{in} and larger $A_{IN,A}$ on a Square clock signal yields lower current consumption
(3) Required for stable internal clock signal
(4) Typical value very dependant on input clock signal. Lower f_{in}, $V_{IH,D}$ at maximum and $V_{IL,D}$ at minimum on a Square clock signal yields lower current consumption

The switch from analog to digital mode is controlled by the host software and selected per application.

Figure 5-2 ICA ANALOG input characteristics



Note: 1:$V_{IN,A\_max.}$ must be below VDD_IO
2:$V_{IN,A\_min.}$ must be above 0
3:$A_{IN,A}$ should be between 0.2V and VDD_LP
4:The switching point for the ICA amplifier to consider the CLK high or low is related to the V_{IN,A_DC} level of the CLK signal, i.e. the CLK DC level
5:The CLK is shown here as a clipped triangle for illustration purposes but sine, clipped sine and square is also valid as CLK signal.
6:The T_{CLK} period must be less than 1/10MHz = 100ns and more than 1/ 40MHz=25ns

5.5 Current Consumption

5.5.1 Internal Digital Power Consumption

Table 5-7 Current Consumption on all Digital Supplies in Different Operating Modes

Parameters	min.	typ.	max.	Unit	Test Conditions
IC Off		0			No Power Applied
Power Down		10		µA	No timing available. RTCCLK needs to be applied
Low Power Standby		15		µA	Standby Counter @ RTCCLK
Software Only Standby		25		mA	VDD_PLL & VDD_CORE on
Reduced Processing Mode		100		mA	Correlator blocks running
Full Processing Mode		150		mA	Correlator blocks running

Note: For a description of the power modes see ***Table 4-2***

5.5.2 Internal RF Power Consumption

Table 5-8 Current Consumption of RF Parts

Parameters	min.	typ.	max.	Unit	Test Conditions
RF regulator		2.5		mA	VDD_RFREGIN=2.1V - 3.6V
RF LNA		**10**		mA	VDD_LNA=1.8V, LNA_ON=1
RF PLL		**10**		mA	VDD_RFPLL=1.8V, PLL_ON=1
Remaining Rx path		**30**		mA	VDD_RF=1.8V,REC_ON=1
Total RF (ex Reg)		50		mA	VDD_RF=1.8V
Leakage current when using internal regulator		**5**		µA	VDD_RFREG_IN=3.6V All blocks disabled.
Leakage current without regulator		**10**		µA	VDD_RF and VDD_LNA=1.8V All blocks disabled.

5.6 Current Consumption of Different Voltage Domains

5.6.1 Typical Current Consumption of Digital Voltage Domains

Table 5-9 Typical Current Consumption of Digital Voltage Domains

Parameters	VDD_CORE	VDD_PLL	VDD_LP	VDD_IO	Unit	Test Conditions
IC Off	0	0	0	0		
Deep Power Down	0	0	500	(1)500	nA	Sample Tested
Low Power Standby	0	0	5	5	µA	
Standby	0	0	10	5	µA	ICA in Digital Mode
Power Saving	15	5	<1	<5	mA	
48MHz Operation	90	5	<1	<5	mA	All correlators active
72MHz Operation	140	5	<1	<5	mA	All correlators active

Note: (1) Inputs and outputs set in the state that consumes the least power, dependent on I/O type.

5.6.2 Internal Current Consumption of Digital Regulators

Table 5-10 Internal Current Consumption of Digital Regulators

Symbol	Parameters	typ.	max.	Unit	Test Conditions	
					I_{OUT}	Reg In Voltage
$I_{INT\_LP\_Reg}$	Low Power Regulator		15	µA	≤1.4mA	1.7V - 3.6V
$I_{INT\_PLL\_Reg\_Off}$	PLL Regulator (Off)		<1	µA	Off(1)	1.7V - 3.6V
$I_{INT\_PLL\_Reg}$	PLL Regulator		100	µA	≤5mA	1.7V - 3.6V
$I_{INT\_CORE\_Reg\_Off}$	Core Regulator (Off)	<0.01	<3.5	µA	Off(1)	1.7V - 2.5V
$I_{INT\_CORE\_Reg}$	Core Regulator		2.5	mA	≤200mA	1.7V - 2.5V

Note: (1)For these tests, V_{IN} = Max, V_{OUT} = GND

To obtain the total power consumption in operational different modes add together the currents from the appropriate row in **Table 5-8** and **Table 5-9** to the appropriate regulator(s) in **Table 5-10** (if used) then multiply the sum by the appropriate input voltage(s).

The power consumption of a regulator in itself is obtained by adding the loss in the series element in the regulator, $(V_{reg\_in}-V_{reg\_out})*I_{out}$ (where I_{out} is the current that the circuit is

drawing from the regulator), to the internal power consumption required to drive the regulator, V_{reg_in}*$I_{INT.}$

5.7 Regulator Characteristics

5.7.1 Regulator Limits(DC)

Table 5-11 Regulator Limits (DC)

	V_{IN} (Range)	V_{OUT} (1.5V)	I_{OUT} (max)	C_{EXT} (min.)	Notes
Low Power Regulator	1.7-3.6	±6%	1.4mA	68nF	
PLL Regulator	1.7-3.6	±6%	5mA	68nF	
Core Regulator	1.7-2.5	±6%	200mA	5*68nF	Recommended capacitor at Core Regulator input 1µF

5.7.2 Regulator Limits (Dynamic)

Table 5-12 Regulator Limits (Dynamic)

	$T_{STARTUP}$	PSR @		(1) Startup Overshoot	(2)Maximum Overshoot	(3) Settling Time
		DC	2MHz			
Low Power Regulator	<1ms	>40dB	>20dB	<100mV	<100mV	
PLL Regulator	<1ms	>40dB	>20dB	<100mV	<100mV	<350µs
Core Regulator	<1ms	>40dB	>13dB	<10mV	<50mV	<250µs

Note: (1) With recommended capacitances. This adds to other offsets.

Note: (2) With recommended capacitances. At full Load Step. This adds to other offsets.

Note: (3) With recommended capacitances. At full Load Step.

5.8 RF parameters

5.8.1 Noise performance

Table 5-13 System noise performance

Parameter	min.	typ.	max.	unit	comment
System noise figure, from 1st LNA input to ADC outputs.		2.0		dB	

5.8.2 Internal LNA

Table 5-14 LNA parameters

Parameter	min.	nom.	max.	unit	comment
Gain		17		dB	
Noise Figure		1.5	2.0	dB	
1dB compression	-27	-25	-23	dBm	matched input and output @ GPS frequency
1dB compression(915MHz)		-25		dBm	
1dB compression(1710MHz)		-25		dBm	

5.8.3 2nd LNA, Mixer and IF filter.

Table 5-15 2nd LNA, mixer and filter parameters

Parameter	min.	nom.	max.	unit	comment
1dB compression		-27		dBm	matched input @ GPS frequency
1dB compression(915MHz)		-27		dBm	
1dB compression(1710MHz)		-27		dBm	

5.8.4 PGC amplifier

Table 5-16 PGC amplifier and AGC loop parameters

Parameter	min.	nom.	max.	unit	comment
Max added gain in front of 1st LNA		16		dB	Max added external gain that the PGC can compensate for.

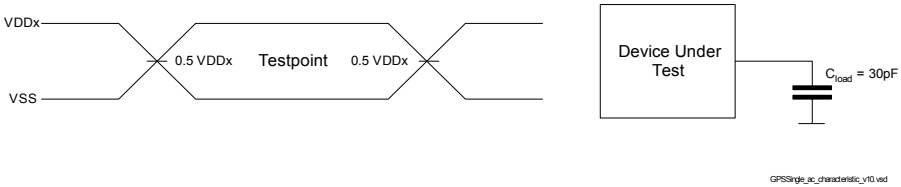
5.9 AC Characteristics

Supply voltage is defined individually for each interface.

Timing measurements are made at 50% of the supply voltage for a rising edge (logic 0 to 1) and a falling edge (logic 1 to 0).

The AC testing input/output waveform is shown in **Figure 5-3**.

Figure 5-3 Input/Output Waveform for AC Tests



5.9.1 UART Chip Select Timing

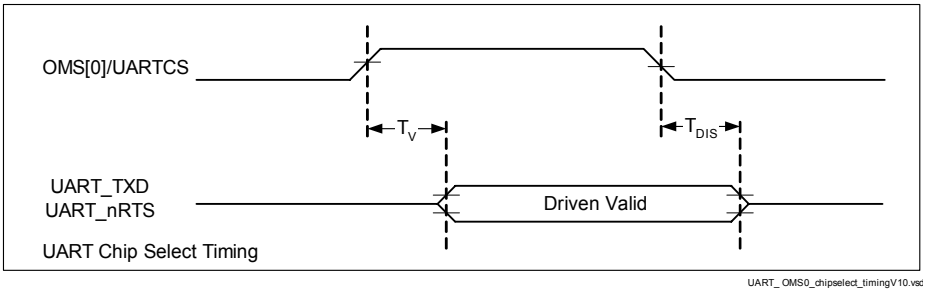


Figure 5-4 Uart chip select timing

Table 5-17 UART Chip Select Timing

Parameter	Description	Min.	Max.	Unit
T_V	UART_TXD/UART_nRTS outputs valid	-	30	ns
T_{DIS}	UART_TXD/UART_nRTS output disable time	-	30	ns

5.9.2 I²C F/S Mode Timing

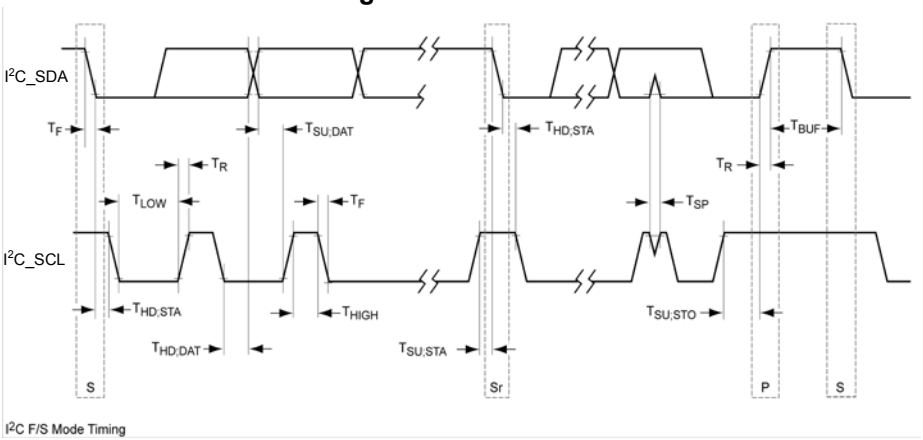


Figure 5-5 I²C F/S Mode Timing

Table 5-18 I²C F/S Mode Timing (1)

Parameter	Description	Fast Mode		Units
		Minimum	Maximum	
FSCL	I²C_SCL clock frequency	0	400	kHz
THD;STA	Hold time (repeated START condition. After this period, the first clock pulse is generated	0.6		µs
TLOW	LOW period of the I²C_SCL clock	1.3		µs
THIGH	HIGH period of the I²C_SCL clock	0.6		µs
TSU;STA	Set-up time for a repeated START condition	0.6		µs
THD;DAT	Data hold time for I2C bus devices	0 (2)	0.9 (3)	µs
TSU;DAT	Data set-up time	100 (4)		ns
TR	Rise time of both the I²C_SDA and the I²C_SCL signal	$20+0.1C_B$	300	ns
TF	Fall time of the I²C_SDA and the I²C_SCL signal	$20+0.1C_B$ (6)	300	ns
TSU;STO	Set-up time for STOP condition	0.6		µs
TBUF	Bus free time between a STOP and a START condition	1.3		µs

Table 5-18 I²C F/S Mode Timing (1)

Parameter	Description	Fast Mode		Units
		Minimum	Maximum	
TOF_I2C	Output fall time from VIH (min) to VIL (max) with a bus capacitance from 10 pF to 400 pF	$20+0.1C_B$ (6)	250	ns

Notes:
1. All values are referenced to minimum (VIH) and maximum (VIL) levels.
2. A device must internally provide a hold time of at least 300 ns for the I^2C_SDA signal (referenced to the minimum VIH level of the I^2C_SCL signal) to bridge the undefined region of the falling edge of I^2C_SCL.
3. The maximum THD;DAT must be met since Hammerhead does not stretch the LOW period (TLOW) of the SCL signal.
4. Measured with a 50 pF load.
5. A Fast Mode I2C bus device can be used in a Standard Mode I2C bus system, but the requirement TSU;DAT 250 ns must be met. This applies automatically since Hammerhead does not stretch the LOW period of the SCL signal.
6. CB = total capacitance of one bus line in pF.

5.9.3 SPI Mode timing

The SPI interface has four different clocking modes and the Hammerhead supports SPI Mode 0 (CPOL=0, CPHA=0). The detailed timing is shown in the following figure:

Figure 5-6 Detailed SPI timing

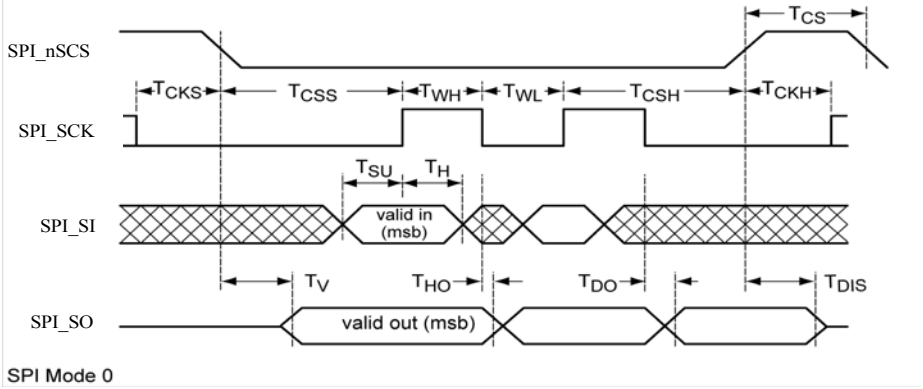


Table 5-19 Detailed SPI Timing (Mode 0)

Parameter	Description	Minimum	Maximum	Units
T_{CKH}	SPI_SCK hold time	0	-	ns
T_{CKS}	SPI_SCK setup time	0	-	ns
T_{CS}	SPI_nSCS de-asserted between SPI cycles	$3 \times T_{CLK}$ [1)]	-	ns
T_{CSS}	SPI_nSCS setup time	$(4 \times T_{CLK}$ [1)]$) + 45 +$ master's setup time	-	ns
T_{CSH}	SPI_nSCS hold time	$T_{WL}/2$	-	ns
T_{WL}	SPI_SCK low time	$(4 \times T_{CLK}$ [1)]$) + 45 +$ master's setup time	-	ns
T_{WH}	SPI_SCK high time	$(2 \times T_{CLK}$ [1)]$) + 20$	-	ns
T_{SU}	SPI_SI setup time	15	-	ns
T_{H}	SPI_SI hold time	5	-	ns
T_{V}	SPI_SO output valid	--	35	ns
T_{HO}	SPI_SO hold time	T_{CLK} [1)]	-	ns

Table 5-19 Detailed SPI Timing (Mode 0)

Parameter	Description	Minimum	Maximum	Units
T_{DO}	SPI_SO output valid	--	$(4 \times T_{CLK}$[1)$) + 45$	ns
T_{DIS}	SPI_SO output disable time	--	35	ns

1) Tclk refers to the clock period of the CLK pin

5.9.4 Boundary Scan Timing

Figure 5-7 Boundary Scan Timing: Explanation of Parameters.

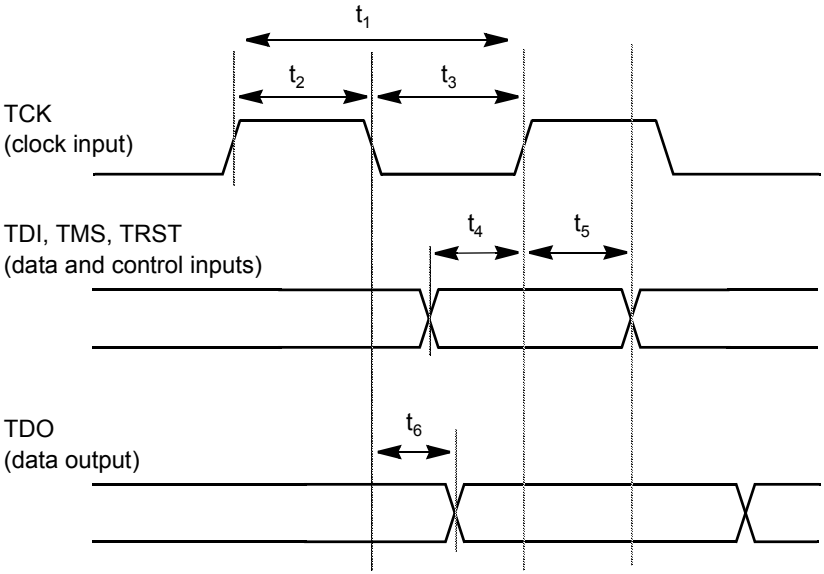


Table 5-20 Boundary Scan Timing: Applications with Enabled I2C Interface

Symbol	Parameter Description	Limit Values			Unit
		min.	typ.	max.	
t_1	TCK clock period	1000			ns
t_2	TCK clock period low	400			ns
t_3	TCK clock period high	400			ns
t_4	TMS / TDI setup time to TCK	10			ns

Table 5-20 Boundary Scan Timing: Applications with Enabled I2C Interface

Symbol	Parameter Description	Limit Values			Unit
		min.	typ.	max.	
t_5	TMS / TDI hold time from TCK	5			ns
t_6	TCK low to TDO valid			25	ns

Table 5-21 Boundary Scan Timing: Applications with Disabled I2C Interface

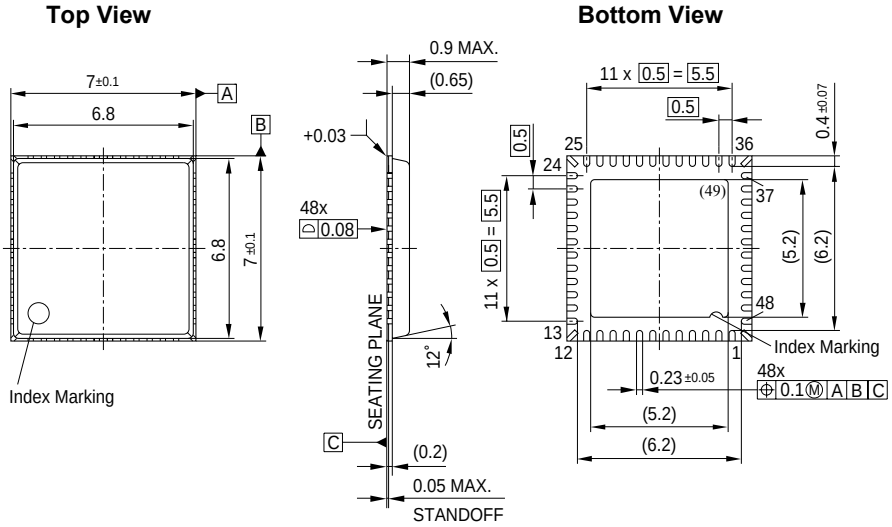
Symbol	Parameter Description	Limit Values			Unit
		min.	typ.	max.	
t_1	TCK clock period	100			ns
t_2	TCK clock period high	40			ns
t_3	TCK clock period low	40			ns
t_4	TMS / TDI setup time to TCK	10			ns
t_5	TMS / TDI hold time from TCK	5			ns
t_6	TCK low to TDO valid			25	ns

Recommendation: TCK should have a 50% duty cycle.

6 Package

6.1 Package Outline

Figure 6-1 Package Outline PG-VQFN-48-4



Ground is connected to the exposed bottom pad (49).

Table 6-1 Typical Package Dimensions

Package	x (mm)	y (mm)	z (mm)	Pitch (mm)
PG-VQFN-48-4	7.0	7.0	0.9	0.5

6.2 Package footprint

Figure 6-2 Package footprint

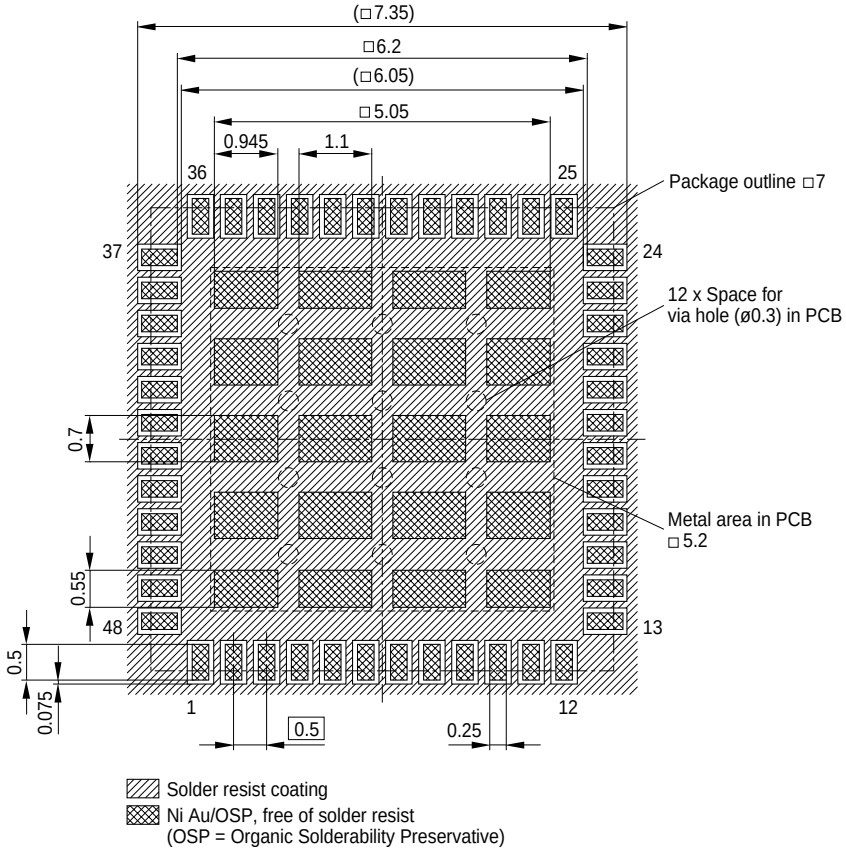


Table 6-2 Thermal Characteristics.

Symbol	max	Unit	Conditions
R_{thJA}	25	C/W	P_V=1W Exposed bottom pad soldered to 4 layer PCB with vias

6.3 Links to more information

Recommendations for Printed Circuit Board Assembly of Infineon P-VQFN Packages

Figure 6-3

7 Appendix A Package and handling

7.1 Storage, baking and handling

See IPC/JEDEC J-STD-033A level 3.

7.2 ESD sensitivity

See Qualification Report

7.3 Moisture Sensitivity Level

See Qualification Report

7.4 Peak package temperature level

See Qualification Report

8 Appendix C S-parameters

Table 8-1 First LNA unmatched

Frequency	S11		S22	
	Mag.	Phase	Mag.	Phase
1575				

Table 8-2 First LNA noise matched

Frequency	S11		S22	
	Mag.	Phase	Mag.	Phase
1575				

Table 8-3 Second LNA unmatched

Frequency	S11		S22	
	Mag.	Phase	Mag.	Phase
1575			N/A	N/A